Intel® 82854 Graphics Memory Controller Hub (GMCH)

Datasheet

Revision 2.0

June 2005

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Revision History

Date	Revision	Description
March 2005	1.0	Initial release of this document.
June 2005	2.0	Add support for Genuine Intel® Processor at 1.2 GHz and Genuine Intel® Processor at 1.5 GHz technology.

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1.0 Introduction

This document is the datasheet for the Intel® 82854 Graphics Memory Controller Hub (GMCH).

1.1 Overview

The Intel® 854 chipset is a combination of the Intel® 82854 Graphics Memory Controller Hub (GMCH) (Graphics Memory Controller Hub) and ICH4-M (I/O Controller Hub). The Intel 854 Chipset is designed to work with the Ultra Low Voltage (ULV) Intel® Celeron® M processor at 600 MHz with 512 KB of on-die L2 cache on an 0.13 micron process, Genuine Intel® Processor at 1.2 GHz, and Genuine Intel® Processor at 1.5 GHz. The Intel® 82854 GMCH provides high-performance, integrated graphics and manages the flow of information. Figure 1 depicts the Intel 854 chipset block diagram.

Processor/Host Bus Support

The Genuine Intel® Processor at 1.2 GHz and Genuine Intel® Processor at 1.5 GHz have the following key features:

- High performance, low power core
- AGTL+ bus driver technology with integrated AGTL+ termination resistors and low voltage operation
- Supports Intel Architecture with Dynamic Execution
- 400-MHz, Source-Synchronous processor system bus
- 2x address, 4x data
- On-die, primary 32-Kbyte instruction cache and 32-Kbyte write-back data cache
- On-die, 512-Kbyte second level cache with Advanced Transfer Cache Architecture
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2)
- Advanced Power Management features

Memory System

- Directly supports one DDR SDRAM channel, 64-bits wide
- Supports 266/333-MHz DDR SDRAM devices with max of two, double-sided DIMM (four rows populated) with unbuffered PC2100/PC2700 DDR SDRAM.
- Supports 128-Mbit, 256-Mbit, and 512-Mbit technologies providing maximum capacity of 2 GB with x16 devices
- All supported devices have four banks
- Supports up to 16 simultaneous open pages
- Supports page sizes of 2 kB, 4 kB, 8 kB, and 16 kB. Page size is individually selected for every row
- UMA support only

System Interrupts

- Supports Intel 8259 and front side bus interrupt delivery mechanism
- Supports interrupts signaled as upstream memory writes from PCI and Hub interface
- MSI sent to the CPU through the system bus
- IOxAPIC in ICH4-M provides redirection for upstream interrupts to the system bus

Video Stream Decoder

- Hardware motion compensation for MPEG2
- All video format decoder (18 ATSC video formats) supported
- Dynamic Bob and Weave support for video streams
- Software DVD at 60 Fields/second and 30 frames/second full screen
- Support for standard definition DVD (i.e., NTSC pixel resolution of 720x480, and so on) quality encoding at low CPU utilization

Video Overlay

- Single high quality scalable overlay and second Sprite to support second overlay
- Multiple overlay functionality provided via arithmetic stretch BLT (Block Transfer)
- 5-tap horizontal, 3-tap vertical filtered scaling
- Multiple overlay formats
- Direct YUV from overlay to TV-out
- Independent gamma correction
- Independent brightness / contrast/ saturation
- Independent tint/hue support
- Destination colorkeying
- Source chromakeying

Display

- Analog display support
  - 350-MHz integrated 24-bit RAMDAC that can drive a standard progressive scan analog monitor with pixel resolution up to 1600x1200 at 85 Hz and up to 2048x1536 at 75 Hz
- Dual independent pipe support
  - Concurrent: different images and display timings on each display device
  - Simultaneous: same images and display timings on each display device
- DVO (DVOB and DVOC) support
  - Digital video out ports DVOB and DVOC with 165-MHz dot clock on each 12-bit interface; two 12-bit channels can be combined to form one dual channel 24-bit interface with an effective dot clock of 330 MHz
  - The combined DVO B/C ports as well as individual DVO B/C ports can drive a variety of DVO devices (TV-Out Encoders, TMDS and LVDS transmitters, and so on) with pixel resolution up to 1600x1200 at 85 Hz and up to 2048x1536 at 72 Hz.
  - Compliant with DVI Specification 1.0
- Tri-view support through DVO B, C port, and CRT

Internal Graphics Features

- Up to 64 MB of dynamic video memory allocation
- Display image rotation
- Graphics core frequency at 200, 250 MHz
- 2D graphics engine
  - Optimized 128-bit BLT engine
  - Ten programmable and predefined monochrome patterns
  - Alpha Stretch BLT (via 3D pipeline)
  - Anti-aliased lines
  - Hardware-based BLT Clipping and Scissoring
  - 32-bit Alpha Blended cursor
  - Programmable 64 x 64 3-color Transparent cursor
  - Color Space Conversion
  - Three Operand Raster BLTs
  - 8-bit, 16-bit, and 32-bit color
  - ROP support
  - DIB translation and Linear/Tile addressing
  - Multiple hardware color cursor support (32-bit with alpha and legacy 2-bpp mode)
  - Accompanying I^2C and DDC channels provided through multiplexed interface

- 3D graphics engine
  - — 3D setup and render engine
  - — Enhanced Hardware Binning Instruction Set supported
  - — Zone rendering
  - — High quality performance texture engine
  - — Viewpoint transform and perspective divide
  - — Triangle lists, strips and fans support
  - — Indexed vertex and flexible vertex formats
  - — Pixel accurate fast scissoring and clipping operation
  - — Backface culling support
  - — Direct 3D support
  - — Anti-Aliased lines support
  - — Sprite points support
  - — Provides the highest sustained fill rate performance in 32-bit color and 24-bit W mode
  - — High quality performance texture engine
  - — 266-MegaTexel/s peak performance
  - — Per pixel perspective corrected texture mapping
  - — Single pass texture compositing (multi-textures)
  - — Enhanced texture blending functions
  - — Twelve level of detail MIP map sizes from 1x1 to 2k x 2k
  - — Numerous texture formats
  - — Alpha and Luminance maps
  - — Texture chromakeying
  - — Bilinear, trilinear, and anisotropic MIP map filtering
  - — Cubic environment reflection mapping
  - — Dot product bump-mapping
  - — Embossed bump-mapping
  - — DXTn texture decompression
  - — FX1 texture compression
  - — 3D graphics rasterization enhancements
  - — One Pixel per clock
  - — Flat and Gouraud shading
  - — Color alpha blending for transparency
  - — Vertex and programmable pixel fog and atmospheric effects
  - — Color specular lighting
  - — Z Bias support

- Dithering
- Line and full-scene anti-aliasing
- 16- and 24-bit Z buffering
- 16- and 24-bit W buffering
- 8-bit Stencil buffering
- Double and triple render buffer support
- 16- and 32-bit color
- Destination alpha
- Vertex cache
- Optimal 3D resolution supported
- Fast Clear support
- ROP support

Hub Interface to ICH4-M

- 266-MB/s point-to-point Hub interface to ICH4-M
- 66-MHz base clock

Graphic Power Management

- Dynamic Frequency Switching
- Memory Self-Refresh during C3
- Intel Display Power Saving Technology

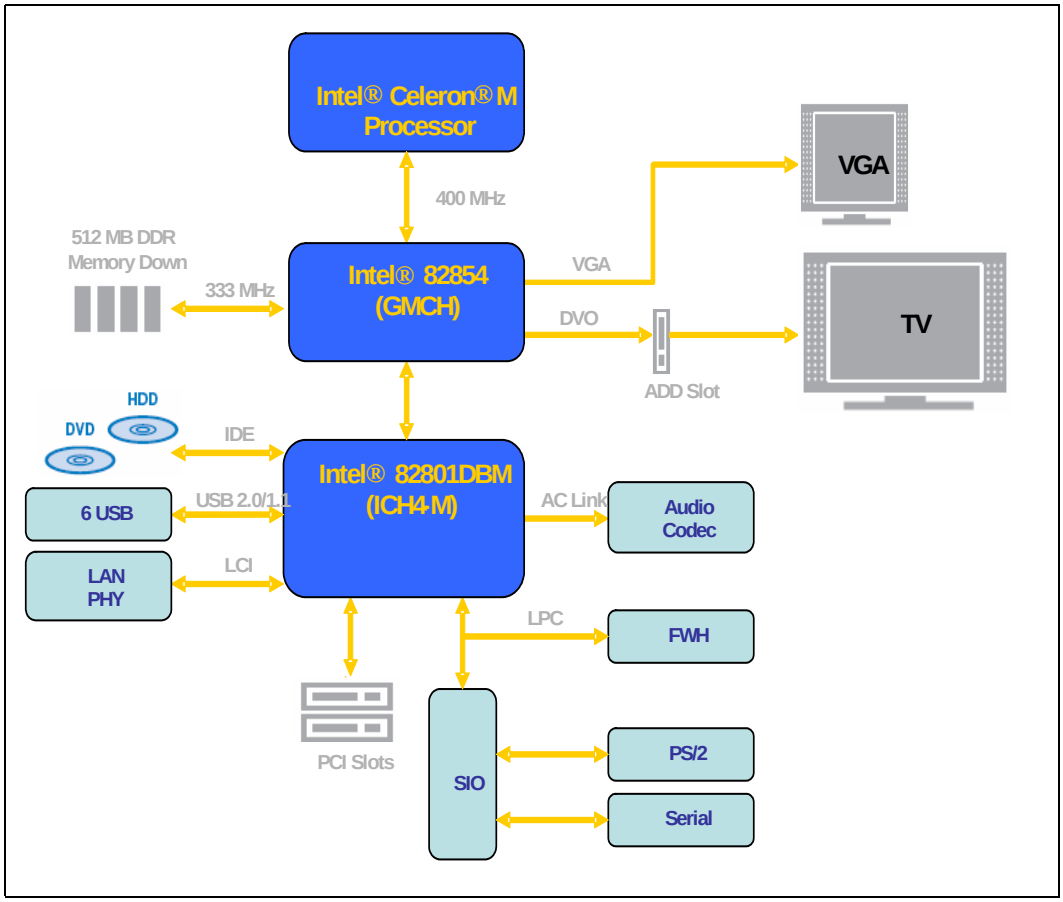
Power Management

- SMRAM space remapping to A0000h (128-kB)
- Supports extended SMRAM space above 256-MB, additional 1-MB TSEG from top of memory, cacheable (cacheability controlled by CPU)
- APM Rev 1.2 compliant power management
- Supports Suspend to System Memory (S3), Suspend to Disk (S4) and Soft Off (S5)
- ACPI 1.0b, 2.0 support
- Optimized Clock Gating for 3D and Display Engines
- On-Die Thermal Sensor

Package

732-pin Micro-FCBGA (37.5 x 37.5 mm)

Figure 1. Intel® 854 Chipset system block diagram (Native Graphic mode)



1.2 Terminology

Table 1. Terms and Descriptions

Term	Description
AGTL+	Advanced Gunning Transceiver Logic + (AGTL+) bus
BLI	Backlight Inverter
Core	The internal base logic in the Intel® 82854 GMCH
CPU	Central Processing Unit
CRT	Cathode Ray Tube
DBI	Dynamic Bus inversion
DBL	Display Brightness Link
DDC	Display Data Channel (standard created by VESA)
DPMS	Display Power Management Signaling (standard created by VESA)
DVI*	Digital Visual Interface is the interface specified by the DDWG (Digital Display Working Group) DVI Spec. Rev. 1.0 utilizing only the Silicon Image developed TMDS protocol
DVMT	Dynamic Video Memory Technology
DVO	Digital Video Out
EDID	Extended Display Identification Data
EIST	Enhanced Intel® SpeedStep® Technology
FSB	Front side bus. Connection between Intel® 82854 GMCH and the CPU. Also known as the Host interface
Full Reset	A full Intel® 82854 GMCH Reset is defined in this document when RSTIN# is asserted
GMCH	Refers to the GMCH component. Throughout this datasheet, the Intel® 82854 Graphics Memory Controller Hub (GMCH) will be referred to as the GMCH.
HD	High definition, typically MP@HL for MPEG2; Resolution supported are 720p, 1080i and 1080p
Host	This term is used synonymously with processor
Hub Interface (HI)	The proprietary interconnect between the Intel® 82854 GMCH and the ICH4-M component. In this document, the Hub interface cycles originating from or destined for the ICH4-M are generally referred to as “Hub interface cycles.” Hub cycles originating from or destined for the primary PCI interface on are sometimes referred to as “Hub interface/PCI cycles”
I^2C	Inter-IC (a two wire serial bus created by Philips)
IGD	Integrated Graphics Device

Intel 82801DBM ICH4-M	The component contains the primary PCI interface, LPC interface, USB 2.0, ATA-100, AC'97, and other I/O functions. It communicates with the Intel® 82854 GMCH over a proprietary interconnect called the Hub interface. Throughout this datasheet, the Intel 82801DBM ICH4-M component will be referred to as the ICH4-M
IPI	Inter Processor Interrupt
LCD	Liquid Crystal Display
MSI	Message Signaled Interrupts. MSI allow a device to request interrupt service via a standard memory write transaction instead of through a hardware signal
Native Graphic Mode	The Intel® 82854 GMCH can support RGB and Dual Independent Display in this mode
PWM	Pulse Width Modulation
SD	Standard definition, typically MP@ML for MPEG2
SSC	Spread Spectrum Clocking
STB	Set Top Box
System Bus	Processor-to-Intel® 82854 GMCH interface. The Enhanced mode of the Scalable bus is the P6 Bus plus enhancements, consisting of source synchronous transfers for address and data, and system bus interrupt delivery. The Intel Celeron M processor implements a subset of Enhanced mode.
UMA	Unified Memory Architecture with graphics memory for the IGD inside system memory
VDL	Video Data Link

1.3 Reference Documents

Table 2. Reference Documents

Document	Location
Intel® Celeron® M Processor Datasheet	http://www.intel.com/design/mobile/datashts/300302.htm
Ultra Low Voltage Intel(R) Celeron(R) M Processor at 600 MHz Addendum to the Intel(R) Celeron(R) M Processor Datasheet	http://developer.intel.com/design/intarch/datashts/301753.htm
Intel® 854 Chipset Platform Design Guide for Use with Ultra Low Voltage Intel® Celeron® M Processor at 600 MHz	Please contact your local Intel representative for this document.
PCI Local Bus Specification 2.2	http://www.pcisig.com
Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Datasheet	http://developer.intel.com/design/mobile/datashts/252337.htm
Advanced Configuration and Power Management (ACPI) Specification 1.0b & 2.0	http://www.acpi.info/
IA-32 Intel® Architecture Software Developer Manual Volume 3: System Programming Guide	http://developer.intel.com/design/pentium4/manuals/245472.htm
INTEL® DIGITAL VIDEO OUT (DVO) PORT HARDWARE EXTERNAL DESIGN SPECIFICATION (EDS) VER – 2.X	Please contact your local Intel representative for this document.
ARIB TR-B15 Operational Guidelines for Digital Satellite Broadcasting (detailed Implementation guideline for receiver)	http://www.arib.or.jp/english/html/overview/ov/tr_b15.html
ATSC Standards	http://www.atsc.org/standards.html

2.0 Intel® 82854 GMCH Overview

2.1 System Architecture

The Intel® 82854 GMCH includes a processor interface, DDR SDRAM interface, display interface, and Hub interface.

Combined with the ULV Intel® Celeron® M Processor or Genuine Intel® Processor, and an ICH4-M, it provides many of the functions required to deliver the features below:

- Overall system software platform
- Graphic overlay function for the GUI and 3-D graphics for gaming.
- Soft CODEC function
- STB middleware execution
- New STB embedded applications requiring IA level of high performance.

2.1.1 Intel® 82854 GMCH

The Intel® 82854 GMCH is in a 732-pin Micro-FCBGA package that contains the following functionality listed below:

- AGTL+ host bus supporting 32-bit host addressing with Enhanced Intel SpeedStep technology support
- Supports a single channel of DDR SDRAM memory
- System memory supports DDR 266/333 MHz (SSTL_2) DDR SDRAM
- Integrated graphics capabilities: Graphic Core frequency at 200, 250 MHz
- Supports three display ports: one progressive scan analog monitor and two DVO ports.
- Enhanced Power Management Graphics features

2.2 Processor Host Interface

The Intel® 82854 GMCH supports the Intel Celeron M Processor, and Genuine Intel Processor.

Key features of the front side bus (FSB) are:

- Support for a 400-MHz system bus frequency.
- Source synchronous double pumped address (2X)
- Source synchronous quad pumped data (4X)
- Front side bus interrupt delivery
- Low voltage swing Vtt (1.05 ~ 1.55V)
- Dynamic Power Down (DPWR#) support
- Integrates AGTL+ termination resistors on all of the AGTL+ signals
- Supports 32-bit host bus addressing allowing the CPU to access the entire 4 GB of the GMCH memory address space.
- An 8-deep, In-Order queue
- Support DPWR# signal
- Supports one outstanding defer cycle at a time to any particular I/O interface

2.3 GMCH System Memory Interface

The GMCH system memory controller directly supports the following:

- One channel of PC2100/2700 DIMM DDR SDRAM memory
- DDR SDRAM devices with densities of 128-Mb, 256-Mb, and 512-Mb technology
- Up to 1 GB (512-Mb technology) with two DDR DIMMs
- Up to 2 GB (512-Mb technology) using high density devices with two DDR DIMMs

Table 3. DDR SDRAM Memory Capacity

Technology	Width	System Memory Capacity	System Memory Capacity with Stacked Memory
128 Mb	16	256 MB	-
256 Mb	16	512 MB	-
512 Mb	16	1 GB	-
128 Mb	8	256 MB	512 MB
256 Mb	8	512 MB	1 GB
512 Mb	8	1 GB	2 GB

The GMCH system memory interface supports a thermal throttling scheme to selectively throttle reads and/or writes. Throttling can be triggered either by the on-die thermal sensor, or by preset write bandwidth limits. Read throttle can also be triggered by an external input pin. The memory controller logic supports aggressive Dynamic Row Power Down features to help reduce power and supports Address and Control line tri-stating when DDR SDRAM is in an active power down or in self refresh state.

The GMCH system memory architecture is optimized to maintain open pages (up to 16-KB page size) across multiple rows. As a result, up to 16 pages across four rows is supported. To complement this, the GMCH will tend to keep pages open within rows, or will only close a single bank on a page miss. The GMCH supports only four bank memory technologies.

2.4 Graphics Features

The GMCH IGD provides a highly integrated graphics accelerator delivering high performance 2D, 3D, and video capabilities. With its interfaces to UMA using a DVMT configuration, an analog display, and two digital display ports, the GMCH can provide a complete graphics solution.

The GMCH also provides 2D hardware acceleration for block transfers of data (BLTs). The BLT engine provides the ability to copy a source block of data to a destination and perform raster operations (for example, ROP1, ROP2, and ROP3) on the data using a pattern, and/or another destination. Performing these common tasks in hardware reduces CPU load, and thus improves performance.

High bandwidth access to data is provided through the system memory interface. The GMCH uses Tiling architecture to increase system memory efficiency and thus maximize effective rendering bandwidth. The Intel® 82854 GMCH improves 3D performance and quality with 3D Zone rendering technology. The Intel® 82854 GMCH also supports Video Mixer rendering, and Bi-Cubic filtering.

2.5 Display Features

The Intel® 82854 GMCH has three display ports: one analog and two digital. With these interfaces, the GMCH can provide support for a progressive scan analog monitor and two DVO ports. The native graphic mode is able to deliver up to two streams of data via the two DVO ports.

2.5.1 GMCH Analog Display Port

The Intel® 82854 GMCH has an integrated 350-MHz, 24-bit RAMDAC that can directly drive a progressive scan analog monitor pixel resolution up to 1600x1200 at 85-Hz refresh and up to 2048x1536 at 75-Hz refresh. In the native graphic mode, the Analog display port can be driven by Pipe A or Pipe B.

2.5.2 GMCH Integrated DVO Ports

The Intel® 82854 GMCH provides a digital display channel that is capable of driving a pixel clock up to 165 MHz.

The GMCH supports three ARIB planes of graphics: Still Picture Plane, Text and Graphic Plane, and Superimpose Text Plane at a frame rate of 10 fps. A minimum of two displays are supported. The ARIB plane resolutions supported can be found in Figure 8.

In native graphics mode, the GMCH supports a single display up to 60 fps real time with maximum resolution of 720 x 480 pixels.

2.6 Hub Interface

A proprietary interconnect connects the GMCH to the ICH4-M. All communication between the GMCH and the ICH4-M occurs over the Hub interface 1.5. The Hub interface runs at 66 MHz (266-MB/s).

2.7 Address Decode Policies

Host initiated I/O cycles are positively decoded to the GMCH configuration space and subtractively decoded to the Hub interface. Host initiated system memory cycles are positively decoded to DDR SDRAM and are again subtractively decoded to the Hub interface, if less than 4 GB. System memory accesses from the Hub interface to DDR SDRAM will be snooped on the FSB.

2.8 GMCH Clocking

The GMCH has the following clock input/output pins:

- 400-MHz, spread spectrum, low voltage differential BCLK, BCLK# for front side bus (FSB)
- 66-MHz, 3.3-V GCLKIN for Hub interface buffers
- Six pairs of differential output clocks (SCK[5:0], SCK[5:0]#), 200/266 MHz, 2.5 V for system memory interface
- 48-MHz, non-Spread Spectrum, 3.3-V DREFCLK for the Display Frequency Synthesis
- 8-MHz or 66-MHz, Spread Spectrum, 3.3-V DREFSSCLK for the Display Frequency Synthesis
- Up to 148.5 MHz, 1.5-V DVOBCCLKINT for TV-Out mode
- DPMS clock for S1-M

Clock Synthesizer chips are responsible for generating the system host clocks, GMCH display clocks, Hub interface clocks, PCI clocks, SIO clocks, and FWH clocks. The host target speed is 400 MHz. The GMCH does not require any relationship between the BCLK Host clock and the 66-MHz clock generated for the Hub interface; they are asynchronous to each other. The Hub interface runs at a constant 66-MHz base frequency. Table 4 indicates the frequency ratios between the various interfaces that the GMCH supports.

Table 4. Intel® 82854 GMCH Interface Clocks

Interface	Clock Speed	CPU System Bus Frequency Ratio	Samples Per Clock	Data Rate (Mega-samples/s)	Data Width (Bytes)	Peak Bandwidth (MB/s)
CPU Bus	100 MHz	Reference	4	400	8	3200
DDR SDRAM	133 MHz	1:1 Synchronous	2	266	8	2128
	166 MHz	1:1 Synchronous	2	333	8	2664
DVO B or DVO C (Native Graphic Mode)	Up to 165 MHz	Asynchronous	2	330	1.5	495
DVO B+DVO C (Native Graphic Mode)	Up to 330 MHz	Asynchronous	2	660	3	1980
DAC Interface	350 MHz	Asynchronous	1	350	3	1050

2.9 System Interrupts

The GMCH supports both the legacy Intel 8259 Programmable Interrupt delivery mechanism and the Intel Celeron M processor FSB interrupt delivery mechanism. The serial APIC Interrupt mechanism is not supported.

The Intel 8259 Interrupt delivery mechanism support consists of flushing in bound Hub interface write buffers when an Interrupt Acknowledge cycle is forwarded from the system bus to the Hub interface.

PCI MSI interrupts are generated as memory writes. The GMCH decodes upstream memory writes to the range 0FEE0_0000h - 0FEEF_FFFFh from the Hub interface as message based interrupts. The GMCH forwards the memory writes along with the associated write data to the system bus as an Interrupt Message transaction. Since this address does not decode as part of main system memory, the write cycle and the write data do not get forwarded to system memory via the write buffer. The GMCH provides the response and HTRDY# for all Interrupt Message cycles including the ones originating from the GMCH. The GMCH also supports interrupt redirection for upstream interrupt memory writes.

For message based interrupts, system write buffer coherency is maintained by relying on strict ordering of memory writes. The GMCH ensures that all memory writes received from a given interface prior to an interrupt message memory write are delivered to the system bus for snooping in the same order that they occur on the given interface.

3.0 Signal Description

This section describes the Intel® 82854 GMCH signals. These signals are arranged in functional groups according to their associated interface. The following notations are used to describe the signal type.

Notation	Description
I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin

The signal description also includes the type of buffer used for the particular signal:

Buffer	Description
AGTL+	Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. The GMCH integrates AGTL+ termination resistors, and supports VTTLF of 1.05 V ± 5%. AGTL+ signals are "inverted bus" style where a low voltage represents a logical 1.
DVO	DVO buffers (1.5-V tolerant)
Hub	Compatible to Hub interface 1.5
SSTL_2	Stub Series Termination Logic compatible signals (2.5-V tolerant)
LVTTL	Low Voltage TTL compatible signals (3.3-V tolerant)
CMOS	CMOS buffers (3.3-V tolerant)
Analog	Analog signal interface
Ref	Voltage reference signal

Note: System Address and Data Bus signals are logically inverted signals. In other words, the actual values are inverted from what appears on the system bus. This must be taken into account and the addresses and data bus signals must be inverted inside the GMCH. All processor control signals follow normal convention: A 0 indicates an active level (low voltage), and a 1 indicates an active level (high voltage).

3.1 Host Interface Signals

Table 5. Host Interface Signal Descriptions

Signal Name	Type	Description
ADS#	I/O AGTL+	**Address Strobe:** The system bus owner asserts ADS# to indicate the first of two cycles of a request phase. The GMCH can assert this signal for snoop cycles and interrupt messages.
BNR#	I/O AGTL+	**Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
BPRI#	O AGTL+	**Bus Priority Request:** The GMCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	I/O AGTL+	**Bus Request 0#:** The GMCH pulls the processor bus BREQ0# signal low during **CPURST#.** The signal is sampled by the processor on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 BCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 BCLKs. BREQ0# should be tristated after the hold time requirement has been satisfied. During regular operation, the GMCH will use BREQ0# as an early indication for FSB Address and Ctl input buffer and sense amp activation.
CPURST#	O AGTL+	**CPU Reset:** The CPURST# pin is an output from the GMCH. The GMCH asserts CPURST# while RESET# (PCIRST# from ICH4-M) is asserted and for approximately 1 ms after RESET# is deasserted. The CPURST# allows the processor to begin execution in a known state. Note that the ICH4-M must provide CPU strap set-up and hold-times around CPURST#. This requires strict synchronization between GMCH, CPURST# deassertion and ICH4-M driving the straps.
DBSY#	I/O AGTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O AGTL+	**Defer:** GMCH will generate a deferred response as defined by the rules of the GMCH's Dynamic Defer policy. The GMCH will also use the DEFER# signal to indicate a CPU retry response.
DINV[3:0]#	I/O AGTL+	**Dynamic Bus Inversion:** Driven along with the HD[63:0]# signals. Indicates if the associated signals are inverted or not. DINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. DINV# Data Bits DINV[3]# HD[63:48]# DINV[2]# HD[47:32]# DINV[1]# HD[31:16]# DINV[0]# HD[16:0]#
DPSLP#	I CMOS	**Deep Sleep #:** This signal comes from the ICH4-M device, providing an indication of C3 and C4 state control to the CPU. Deassertion of this signal is used as an early indication for C3 and C4 wake up (to active HPLL). Note that this is a low-voltage CMOS buffer operating on the FSB VTT power plane.

DRDY#	I/O AGTL+	**Data Ready:** Asserted for each cycle that data is transferred.
HA[31:3]#	I/O AGTL+	**Host Address Bus:** HA[31:3]# connects to the CPU address bus. During processor cycles the HA[31:3]# are inputs. The GMCH drives HA[31:3]# during snoop cycles on behalf of Hub interface. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the CPU bus.
HADSTB[1:0]#	I/O AGTL+	**Host Address Strobe:** HA[31:3]# connects to the CPU address bus. During CPU cycles, the source synchronous strobes are used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate. **Strobe** — **Address Bits** HADSTB[0]# — HA[16:3]#, HREQ[4:0]# HADSTB[1]# — HA[31:17]#
HD[63:0]#	I/O AGTL+	**Host Data:** These signals are connected to the CPU data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the CPU bus.
HDSTBP[3:0]# **HDSTBN[3:0]#**	I/O AGTL+	**Differential Host Data Strobes:** The differential source synchronous strobes are used to **transfer HD[63:0]# and DINV[3:0]# at** the 4x transfer rate. **Strobe** — **Data Bits** HDSTBP[3]#, HDSTBN[3]# — HD[63:48]#, DINV[3]# HDSTBP[2]#, HDSTBN[2]# — HD[47:32]#, DINV[2]# HDSTBP[1]#, HDSTBN[1]# — HD[31:16]#, DINV[1]# HDSTBP[0]#, HDSTBN[0]# — HD[15:0]#, DINV[0]#
HIT#	I/O AGTL+	**Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O AGTL+	**Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I/O AGTL+	**Host Lock:** All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic; that is, no Hub interface snoopable access to system memory is allowed when HLOCK# is asserted by the CPU.
HREQ[4:0]#	I/O AGTL+	**Host Request Command:** Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type. The transactions supported by the GMCH Host Bridge are defined in the Host Interface section of this document.
HTRDY#	O AGTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.

RS[2:0]#	O AGTL+	**Response Status:** Indicates the type of response according to the following the table: **RS[2:0]#** — **Response type** 000 — Idle state 001 — Retry response 010 — Deferred response 011 — Reserved (not driven by GMCH) 100 — Hard Failure (not driven by GMCH) 101 — No data response 110 — Implicit Write back 111 — Normal data response

3.2 DDR SDRAM Interface

Table 6. DDR SDRAM Interface Descriptions

Signal Name	Type	Description
SCS[3:0]#	O SSTL_2	**Chip Select:** These pins select the particular DDR SDRAM components during the active state. **NOTE:** There is one SCS# per DDR-SDRAM Physical DDR DIMM device row. These signals can be toggled on every rising System Memory Clock edge (SCMDCLK).
SMA[12:0]	O SSTL_2	**Multiplexed Memory Address:** These signals are used to provide the multiplexed row and column address to the DDR SDRAM.
SBA[1:0]	O SSTL_2	**Bank Select (Memory Bank Address):** These signals define which banks are selected within each DDR SDRAM row. The SMA and SBA signals combine to address every possible location within a DDR SDRAM device.
SRAS#	O SSTL_2	**DDR Row Address Strobe:** SRAS# may be heavily loaded and requires tw0 DDR SDRAM clock cycles for setup time to the DDR SDRAMs. Used with SCAS# and SWE# (along with SCS#) to define the system memory commands.
SCAS#	O SSTL_2	**DDR Column Address Strobe:** SCAS# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs. Used with SRAS# and SWE# (along with SCS#) to define the system memory commands.
SWE#	O SSTL_2	**Write Enable:** Used with SCAS# and SRAS# (along with SCS#) to define the DDR SDRAM commands. SWE# is asserted during writes to DDR SDRAM. SWE# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs.
SDQ[63:0]	I/O SSTL_2	**Data Lines:** These signals are used to interface to the DDR SDRAM data bus.
SDQS[8:0]	I/O SSTL_2	**Data Strobes:** Data strobes are used for capturing data. During writes, SDQS is centered on data. During reads, SDQS is edge aligned with data. The following list matches the data strobe with the data bytes. There is an associated data strobe (DQS) for each data signal (DQ) and check bit (CB) group. SDQS[7] -> SDQ[63:56] SDQS[6] -> SDQ[55:48] SDQS[5] -> SDQ[47:40] SDQS[4] -> SDQ[39:32] SDQS[3] -> SDQ[31:24] SDQS[2] -> SDQ[23:16] SDQS[1] -> SDQ[15:8] SDQS[0] -> SDQ[7:0]
SCKE[3:0]	O SSTL_2	**Clock Enable:** These pins are used to signal a self-refresh or power down command to the DDR SDRAM array when entering system suspend. SCKE is also used to dynamically power down inactive DDR SDRAM rows. There is one SCKE per DDR SDRAM row. These signals can be toggled on every rising SCK edge.

SMAB[5,4,2,1]	O SSTL_2	**Memory Address Copies:** These signals are identical to SMA[5,4,2,1] and are used to reduce loading for selective CPC(clock-per-command). These copies are not inverted.
SDM[8:0]	O SSTL_2	**Data Mask:** When activated during writes, the corresponding data groups in the DDR SDRAM are masked. There is one SDM for every eight data lines. SDM can be sampled on both edges of the data strobes.
RCVENOUT#	O SSTL_2	**Clock Output:** Reserved, NC.
RCVENIN#	O SSTL_2	**Clock Input:** Reserved, NC.

3.3 Hub Interface Signals

Table 7. Hub Interface Signals

Signal Name	Type	Description
HL[10:0]	I/O Hub	**Packet Data**: Data signals used for HI read and write operations.
HLSTB	I/O Hub	**Packet Strobe**: One of two differential strobe signals used to transmit or receive packet data over HI.
HLSTB#	I/O Hub	**Packet Strobe Complement**: One of two differential strobe signals used to transmit or receive packet data over HI.

3.4 Clocks

Table 8. Clock Signals

Signal Name	Type	Description
Host Processor Clocking		
BCLK **BCLK#**	I CMOS	**Differential Host Clock In:** These pins receive a buffered host clock from the external clock synthesizer. This clock is used by all of the GMCH logic that are in the Host clock domain (Host, Hub and system memory). The clock is also the reference clock for the graphics core PLL. This is a low voltage differential input.
System Memory Clocking		
SCK[5:0]	O SSTL_2	**Differential DDR SDRAM Clock:** SCK and SCK# pairs are differential clock outputs. The crossing of the positive edge of SCK and the negative edge of SCK# is used to sample the address and control signals on the DDR SDRAM. There are 3 pairs to each DDR DIMM.
SCK[5:0]#	O SSTL_2	**Complementary Differential DDR SDRAM Clock:** These are the complimentary differential DDR SDRAM clock signals.
DVO/Hub Input Clocking		
GCLKIN	I CMOS	**Input Clock:** 66-MHz, 3.3-V input clock from external buffer DVO/Hub interface.
DVO Clocking		
DVOBCLK **DVOBCLK#**	O DVO	**Differential DVO Clock Output:** These pins provide a differential pair reference clock that can run up to 165-MHz. DVOBCLK corresponds to the primary clock out. DVOBCLK# corresponds to the primary complementary clock out. DVOBCLK and DVOBCLK# should be left as NC (“Not Connected”) if the DVO B port is not implemented.
DVOCCLK **DVOCCLK#**	O DVO	**Differential DVO Clock Output**: These pins provide a differential pair reference clock that can run up to 165-MHz. DVOCCLK corresponds to the primary clock out. DVOCCLK# corresponds to the primary complementary clock out. DVOCCLK and DVOCCLK# should be left as NC (“Not Connected”) if the DVO C port is not implemented.
DVOBCCLKINT	I DVO	**DVOBC Pixel Clock Input/Interrupt:** This signal may be selected as the reference input to either dot clock PLL (DPLL) or may be configured as an interrupt input. A TV-out device can provide the clock reference. The maximum input frequency for this signal is 148.5 -MHz. DVOBC Pixel Clock Input: When selected as the dot clock PLL (DPLL) reference input, this clock reference input supports SSC clocking for DVO LVDS devices. DVOBC Interrupt: When configured as an interrupt input, this interrupt can support either DVOB or DVOC. DVOBCCLKINT needs to be pulled down if the signal is NOT used.

DPMS	I DVO	**Display Power Management Signaling:** This signal is used only in mobile systems to act as the DREFCLK in certain power management states (i.e., Display Power Down Mode); DPMS Clock is used to refresh video during S1-M. Clock Chip is powered down in S1-M. DPMS should come from a clock source that runs during S1-M and needs to be 1.5 V. So, an example would be to use a 1.5-V version of SUSCLK from ICH4-M.
DAC Clocking		
DREFCLK	I LVTTL	**Display Clock Input:** This pin is used to provide a 48-MHz input clock to the Display PLL that is used for 2D/Video and DAC.

3.5 Internal Graphics Display Signals

The IGD has support for DVOB/C interfaces, and an Analog CRT port.Digital Video Output B (DVOB) Port.

3.5.1 Digital Video Output B (DVOB) Port

Table 9. Digital Video Output B (DVOB) Port Signal Descriptions

Name	Type	Description
DVOBD[11:0]	O DVO	**DVOB Data:** This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOBCLK and DVOBCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the lower 12-bits of pixel data. DVOBD[11:0] should be left as NC (“Not Connected”) if not used.
DVOBHSYNC	O DVO	**Horizontal Sync**: HSYNC signal for the DVOB interface. **DVOBHSYNC** should be left as left as NC (“Not Connected”) if not used.
DVOBVSYNC	O DVO	**Vertical Sync**: VSYNC signal for the DVOB interface. DVOBVSYNC should be left as left as NC (“Not Connected”) if the signal is NOT used when using internal graphics device.
DVOBBLANK#	O DVO	**Flicker Blank or Border Period Indication: DVOBBLANK# is** a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOBBLANK# should be left as left as NC (“Not Connected”) if not used.
DVOBFLDSTL	I DVO	**TV Field and Flat Panel Stall Signal**. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. DVOB TV Field Signal: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. DVOB Flat Panel Stall Signal: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOBFLDSTL needs to be pulled down if not used.

3.5.2 Digital Video Output C (DVOC) Port

Table 10. Digital Video Output C (DVOC) Port Signal Descriptions

Name	Type	Description
DVOCD[11:0]	O DVO	**[Native Graphic Mode]** **DVOC Data**: This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOCCLK and DVOCCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the upper 12-bits of pixel data. **DVOCD[11:0]** should be left as left as NC (“Not Connected”) if not used.
DVOCHSYNC	O DVO	**Horizontal Sync**: HSYNC signal for the DVOC interface. DVOCHSYNC should be left as left as NC (“Not Connected”) if not used.
DVOCVSYNC	O DVO	**Vertical Sync**: VSYNC signal for the DVOC interface. DVOCVSYNC should be left as left as NC (“Not Connected”) if the signal is NOT used when using internal graphics device.
DVOCBLANK#	O DVO	**Flicker Blank or Border Period Indication: DVOCBLANK#** is a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOCBLANK# should be left as left as NC (“Not Connected”) if not used.
DVOCFLDSTL	I DVO	**TV Field and Flat Panel Stall Signal**. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. **DVOC TV Field Signal**: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. **DVOC Flat Panel Stall Signal**: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOCFLDSTL needs to be pulled down if not used.

Table 11. DVOB and DVOC Port Common Signal Descriptions

Name	Type	Description
DVOBCINTR#	I DVO	**DVOBC Interrupt**: This pin is used to signal an interrupt, typically used to indicate a hot plug or unplug of a digital display.
ADDID[7:0]	I DVO	**ADDID[7:0]**: These pins are used to communicate to the Video BIOS when an external device is interfaced to the DVO port. **Note**: Bit[7] needs to be strapped low when an on-board DVO device is present. The other pins should be left as NC. ADDID[0] = 0, Reserve ADDID[0] = 1, the Intel® 82854 GMCH is strapped to operate under Native Graphic Mode For detail of strapping option, please refer to Table 33.
DVODETECT	I DVO	**DVODETECT**: This strapping signal indicates to the GMCH whether a DVO device is present or not. When a DVO device is connected, then DVODETECT = 0.

3.5.3 Analog CRT Display

Table 12. Analog CRT Display Signal Descriptions

Pin Name	Type	Description
VSYNC	O CMOS	**CRT Vertical Synchronization**: This signal is used as the vertical sync signal.
HSYNC	O CMOS	**CRT Horizontal Synchronization**: This signal is used as the horizontal sync signal.
RED	O Analog	**Red (Analog Video Output)**: This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-Ω equivalent load on each pin (that is, a 75-Ω resistor on the board, in parallel with the 75-Ω CRT load).
RED#	O Analog	**Red# (Analog Output):** Tied to ground.
GREEN	O Analog	**Green (Analog Video Output)**: This signal is a CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5-Ω equivalent load on each pin (that is, a 75-Ω resistor on the board, in parallel with the 75- Ω CRT load).
GREEN#	O Analog	**Green# (Analog Output):** Tied to ground.
BLUE	O Analog	**Blue (Analog Video Output)** : This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-Ω equivalent load on each pin (that is, a 75-ohm resistor on the board, in parallel with the 75-Ω CRT load).
BLUE#	O Analog	**Blue# (Analog Output):** Tied to ground.

3.5.4 General Purpose Input/Output Signals

Table 13. GPIO Signal Descriptions

GPIO I/F Total	Type	Comments
RSTIN#	I CMOS	**Reset:** Primary Reset, Connected to PCIRST# of ICH4-M.
PWROK	I CMOS	**Power OK**: Indicates that power to GMCH is stable.
EXTTS_0	I CMOS	**External Thermal Sensor Input:** This signal is an active low input to the GMCH and is used to monitor the thermal condition around the system memory and is used for triggering a read throttle. The GMCH can be optionally programmed to send a SERR, SCI, or SMI message to the ICH4-M upon the triggering of this signal.
LCLKCTLA	O CMOS	**SSC Chip Clock Control:** Can be used to control an external clock chip with SSC control.
LCLKCTLB	O CMOS	**SSC Chip Data Control:** Can be used to control an external clock chip for SSC control.
DDCACLK	I/O CMOS	**CRT DDC Clock:** This signal is used as the DDC clock signal between the CRT monitor and the GMCH.
DDCADATA	I/O CMOS	**CRT DDC Data:** This signal is used as the DDC data signal between the CRT monitor and the GMCH.
MI2CCLK	I/O DVO	**DVO I2C Clock:** This signal is used as the I2C_CLK for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MI2CDATA	I/O DVO	**DVO I2C Data:** This signal is used as the I2C_DATA for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MDVICLK	I/O DVO	**DVI DDC Clock:** This signal is used as the DDC clock for a digital display connector (that is, primary digital monitor). This signal is tri-stated during a hard reset.
MDVIDATA	I/O DVO	**DVI DDC Data:** The signal is used as the DDC data for a digital display connector (that is, the primary digital monitor). This signal is tri-stated during a hard reset.
MDDCDATA	I/O DVO	**DVI DDC Clock:** The signal is used as the DDC data for a digital display connector (that is, the secondary digital monitor). This signal is tri-stated during a hard reset.
MDDCCLK	I/O DVO	**DVI DDC Data:** The signal is used as the DDC clock for a digital display connector (that is, the secondary digital monitor). This signal is tri-stated during a hard reset.

3.6 Voltage References, PLL Power

Table 14. Voltage References, PLL Power

Signal Name	Type	Description
Host Processor		
HXRCOMP	Analog	**Host RCOMP:** Used to calibrate the Host AGTL+ I/O buffers.
HYRCOMP	Analog	**Host RCOMP:** Used to calibrate the Host AGTL+ I/O buffers.
HXSWING	Analog	**Host Voltage Swing (RCOMP reference voltage):** This signal provides a reference voltage used by the FSB RCOMP circuit.
HYSWING	Analog	**Host Voltage Swing (RCOMP reference voltage)**: This signal provides a reference voltage used by the FSB RCOMP circuit.
HDVREF[2:0]	Ref Analog	**Host Data (input buffer) VREF**: Reference voltage input for the data signals of the Host AGTL+ Interface. Input buffer differential amplifier to determine a high versus low input voltage.
HAVREF	Ref Analog	**Host Address (input buffer) VREF**: Reference voltage input for the address signals of the Host AGTL+ Interface. This signal is connected to the input buffer differential amplifier to determine a high versus low input voltage.
HCCVREF	Ref Analog	**Host Common Clock (Command input buffer) VREF**: Reference voltage input for the common clock signals of the Host AGTL+ Interface. This signal is connected to the input buffer differential amplifier to determine a high versus low input voltage.
VTTLF	Power	**FSB Power Supply:** VTTLF is the low frequency connection from the board. This signal is the primary connection of power for GMCH.
VTTHF	Power	**FSB Power Supply:** VTTHF is the high frequency supply. It is for direct connection from an internal package plane to a capacitor placed immediately adjacent to the GMCH. **NOTE:** Not to be connected to power rail.
System Memory		
SMRCOMP	**Analog**	**System Memory RCOMP**: This signal is used to calibrate the memory I/O buffers.
SMVREF_0	**Ref Analog**	**Memory Reference Voltage(Input buffer VREF)**:Reference voltage input for Memory Interface. Input buffer differential amplifier to determine a high versus low input voltage.
SMVSWINGH	**Ref Analog**	**RCOMP reference voltage:** This is connected to the RCOMP buffer differential amplifier and is used to calibrate the I/O buffers.
SMVSWINGL	**Ref Analog**	**RCOMP reference voltage**: This is connected to the RCOMP buffer differential amplifier and is used to calibrate the I/O buffers.
VCCSM	**Power**	Power supply for Memory I/O.
VCCQSM	**Power**	Power supply for system memory clock buffers.
VCCASM	**Power**	Power supply for system memory logic running at the core voltage (isolated supply, not connected to the core).

Hub Interface		
HLRCOMP	Analog	**Hub Interface RCOMP**: This signal is connected to a reference resistor in order to calibrate the buffers.
PSWING	Analog	**RCOMP reference voltage**: This is connected to the RCOMP buffer differential amplifier and is used to calibrate the buffers.
HLVREF	Ref Analog	**Input buffer VREF**: Input buffer differential amplifier to determine a high versus low input voltage.
VCCHL	Power	Power supply for Hub interface buffers
DVO		
DVORCOMP	Analog Analog	**Compensation for DVO**: This signal is used to calibrate the DVO I/O buffers.
GVREF	Ref Analog	**Input buffer VREF**: Input buffer differential amplifier to determine a high versus low input voltage.
VCCDVO	Power	Power supply for DVO.
GPIO		
VCCGPIO	Power	Power supply for GPIO buffers
DAC		
REFSET	Ref Analog	**Resistor Set:** Set point resistor for the internal color palette DAC.
VCCADAC	Power	Power supply for the DAC
VSSADAC	Power	Ground supply for the DAC
IGD		
VCC1_5	Power	Digital power supply.
VCC2_5	Power	Digital power supply
VCCA	Power	Analog power supply.
VSSA	Power	Ground supply
Clocks		
VCCAHPLL	Power	Power supply for the Host PLL.
VCCAGPLL	Power	Power supply for the Hub/DVO PLL.
VCCADPLLA	Power	Power supply for the display PLL A.
VCCADPLLB	Power	Power supply for the display PLL B.
Core		
VCC	Power	Power supply for the core.
VSS	Power	Ground supply for the chip.

4.0 Register Description

4.1 Conceptual Overview of the Platform Configuration Structure

The GMCH and ICH4-M are physically connected by a Hub interface. From a configuration standpoint, the Hub interface is logically PCI bus #0. As a result, all devices internal to the GMCH and ICH4-M appear to be on PCI bus #0. The system's primary PCI expansion bus is physically attached to the ICH4-M and from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and therefore has a programmable PCI Bus number. Note that the primary PCI bus is referred to as PCI_A in this document and is not PCI bus #0 from a configuration standpoint. For the GMCH, the graphics subsystem appears to system software to be a real PCI bus behind PCI-to-PCI bridges, resident as devices on PCI bus #0.

The GMCH contains two PCI devices within a single physical component. The configuration registers for the two devices are mapped as devices residing on PCI bus #0.

Device #0: Host-Hub Interface Bridge/DDR SDRAM Controller. Logically this appears as a PCI device residing on PCI bus #0. Physically, Device #0 contains the standard PCI registers, DDR SDRAM registers, the Graphics Aperture Controller registers, HI Control registers and other GMCH specific registers. Device #0 is divided into the following functions:

Function #0: Host Bridge Legacy registers including Graphics Aperture Control registers, HI Configuration registers and Interrupt Control registers

Function #1: DDR SDRAM Interface Registers

Function #3: Intel Configuration Process Registers

Device #2: Integrated Graphics Controller. Logically this appears as a PCI device residing on PCI bus #0. Physically Device #2 contains the Configuration registers for 2D, 3D, and display functions.

Note: The legacy VGA registers are only supported when the Intel® 82854 GMCH is strapped into Native Graphics Mode.

Table 15 shows the Device # assignment for the various internal GMCH devices.

Table 15. Device Number Assignment

GMCH Function	Bus #0, Device#
Host-Hub interface, DDR SDRAM I/F, Legacy control	Device #0
Integrated Graphics Controller (IGD)	Device #2

4.2 Nomenclature for Access Attributes

Table 16 provides the nomenclature for the access attributes.

Table 16. Nomenclature for Access Attributes

RO	**Read Only**. If a register is Read Only, Writes to this register have no effect.
R/W	**Read/Write**. A register with this attribute can be Read and Written.
R/W/L	**Read/Write/Lock**. A register with this attribute can be Read, Written, and Locked.
R/WC	**Read/Write Clear**. A register bit with this attribute can be Read and Written. However, a Write of a 1 clears (sets to 0) the corresponding bit and a Write of a 0 has no effect.
R/WO	**Read/Write Once**. A register bit with this attribute can be Written to only once after power up. After the first Write, this bit becomes Read Only.
L	**Lock**. A register bit with this attribute becomes Read Only after a Lock bit is set.
Reserved Bits	Some of the GMCH registers described in this section contain Reserved bits. These bits are labeled "Reserved". Software must deal correctly with fields that are Reserved. On Reads, software must use appropriate masks to extract the defined bits and not rely on Reserved bits being of any particular value. On Writes, software must ensure that the values of Reserved bit positions are preserved. That is, the values of Reserved bit positions must first be Read, Merged with the new values for other bit positions and then Written back. Note the software does not need to perform Read, Merge, and Write operations for the Configuration Address register.
Reserved Registers	In addition to Reserved bits within a register, the GMCH contains address locations in the configuration space of the Host-Hub Interface Bridge entity that are marked either "Reserved" or "Intel Reserved". The GMCH responds to accesses to "Reserved" address locations by completing the Host cycle. When a "Reserved" register location is Read, in certain cases, a zero value can be returned ("Reserved" registers can be 8-bit, 16-bit, or 32-bit in size) or a non-zero value can be returned. In certain cases, Writes to "Reserved" registers may have no effect on the GMCH or may cause system failure. Registers that are marked as "Intel Reserved" must not be modified by system software.
Default Value upon a Reset	Upon Reset, the GMCH sets all of its internal configuration registers to predetermined default states. Some register values at Reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DDR SDRAM configurations, operating parameters and optional system features that are applicable, and to program the GMCH registers accordingly.
S	SW Semaphore.

A physical PCI Bus #0 does not exist. The Hub interface and the internal devices in the GMCH and ICH4-M logically constitute PCI Bus #0 to configuration software.

4.3 Standard PCI Bus Configuration Mechanism

The PCI Bus defines a slot based “configuration space” that allows each device to contain up to eight functions with each function containing up to 256, 8-bit configuration registers. The PCI Specification defines two bus cycles to access the PCI Configuration Space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the CPU. Configuration Space is supported by a mapping mechanism implemented within the GMCH. The PCI 2.2 specification defines two mechanisms to access Configuration Space: Mechanism #1 and Mechanism #2. The GMCH supports only Mechanism #1.

The Configuration Access Mechanism makes use of the CONFIG_ADDRESS register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA register (at I/O address 0CFCh though 0CFFh). To reference a Configuration register a Dword I/O Write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI Bus, the device on that bus, the function within the device, and a specific Configuration register of the device function being accessed. CONFIG_ADDRESS[31] must be a 1 to enable a Configuration cycle. CONFIG_DATA then becomes a window into the four Bytes of Configuration Space specified by the contents of CONFIG_ADDRESS. Any Read or Write to CONFIG_DATA will result in the GMCH translating the CONFIG_ADDRESS into the appropriate Configuration cycle.

The GMCH is responsible for translating and routing the CPU’s I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal GMCH Configuration registers and to the Hub interface.

4.4 Routing Configuration Accesses

The GMCH supports one bus interface: the Hub interface. PCI Configuration cycles are selectively routed to this interface. The GMCH is responsible for routing PCI Configuration cycles to the proper interface. PCI configuration cycles to the ICH4-M internal devices, and Primary PCI (including downstream devices) are routed to theICH4-M via the Hub interface.

4.4.1 PCI Bus #0 Configuration Mechanism

The GMCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0, then the Configuration cycle is targeting a PCI Bus #0 device.

The Host-Hub Interface Bridge entity within the GMCH is hardwired as Device #0 on PCI Bus #0.

Configuration cycles to any of the GMCH’s internal devices are confined to the GMCH and not sent over Hub interface. Accesses to disabled GMCH internal devices will be forwarded over the Hub interface as Type 0 Configuration cycles.

4.4.2 Primary PCI and Downstream Configuration Mechanism

If the Bus Number in the CONFIG_ADDRESS is non-zero, the GMCH will generate a Type 1 Hub interface Configuration Cycle. A[1:0] of the Hub interface request packet for the Type 1 configuration cycle will be “01”. This Hub interface configuration cycle will be sent over Hub interface.

If the cycle is forwarded to the ICH4-M via Hub interface, the ICH4-M compares the non-zero Bus Number with the Secondary bus number and Subordinate bus number registers of its PCI-to-PCI bridges to determine if the configuration cycle is meant for Primary PCI, one of the ICH4-M’s Hub interfaces, or a downstream PCI bus.

4.5 Register Definitions

The GMCH contains four sets of software accessible registers accessed via the Host CPU I/O Address Space, and they are as follows:

- **Control registers:** I/O Mapped into the CPU I/O Space, which control access to PCI Configuration Space via Configuration Mechanism #1 in the PCI 2.2 specification.
- **Internal Configuration registers:** residing within the GMCH, they are partitioned into two logical device register sets (“logical” since they reside within the single physical device). The first register set is dedicated to Host-HI Bridge functionality (that is, DDR SDRAM configuration, other chip-set operating parameters and optional features). The second register block is for the integrated graphics functions.
- **Internal Memory Mapped Configuration registers:** reside in the GMCH Device #0.
- **Internal Memory Mapped Configuration registers, Legacy VGA registers, or blending function registers:** reside in the GMCH Device #2 that controls the Integrated Graphics Controller.

The GMCH internal registers (I/O Mapped and Configuration registers) are accessible by the Host CPU. The registers can be accessed as Byte, Word (16-bit), or Dword (32-bit) quantities, with the exception of CONFIG_ADDRESS, which can only be accessed as a Dword. All multi-byte numeric fields use “Little Endian Byte Ordering” (that is, lower addresses contain the least significant parts of the field).

Reserved Bits

Some of the GMCH registers described in this section contain Reserved bits. These bits are labeled “Reserved”. Software must deal correctly with fields that are Reserved. On Reads, software must use appropriate Masks to extract the defined bits and not rely on Reserved bits being any particular value. On Writes, software must ensure that the values of Reserved bit positions are preserved. That is, the values of Reserved bit positions must first be Read, Merged with the new values for other bit positions and then Written back.

Note: The software does not need to perform Read, Merge, and Write operations for the Configuration Address register.

Default Value upon Reset

Upon a Full Reset, the GMCH sets all of its Internal Configuration registers to a predetermined default state. Some register values at Reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the

system initialization software (usually BIOS) to properly determine the DDR SDRAM configurations, operating parameters, and optional system features that are applicable and to program the GMCH registers accordingly.

4.6 I/O Mapped Registers

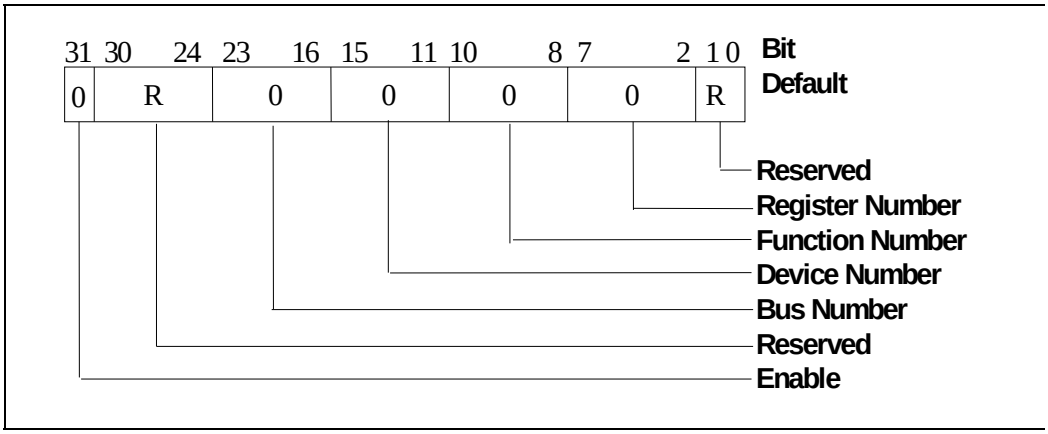
The GMCH contains two registers that reside in the CPU I/O Address Space: the Configuration Address (CONFIG_ADDRESS) Register and the Configuration Data (CONFIG_DATA) Register. The Configuration Address Register enables/disables the Configuration Space and determines what portion of Configuration Space is visible through the Configuration Data window.

4.6.1 CONFIG_ADDRESS – Configuration Address Register

I/O Address:	0CF8h Accessed as a Dword
Default Value:	00000000h
Access:	Read/Write
Size:	32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a Dword. A Byte or Word reference will “pass through” the Configuration Address Register and the Hub interface, onto the PCI bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Figure 2. Configuration Address Register



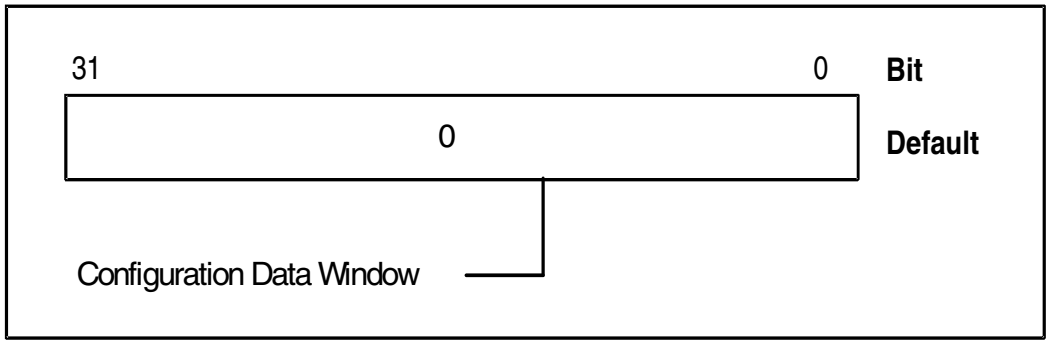
Bit	Descriptions
31	**Configuration Enable (CFGE):** When this bit is set to 1, accesses to PCI Configuration Space are enabled. If this bit is Reset to 0, accesses to PCI Configuration Space are disabled.
30:24	Reserved
23:16	**Bus Number:** When the Bus Number is programmed to 00h, the target of the Configuration Cycle is a Hub interface agent (GMCH, ICH4-M, and so on.). The Configuration Cycle is forwarded to Hub interface if the Bus Number is programmed to 00h and the GMCH is not the target (the device number is >= 2).
15:11	**Device Number:** This field selects one agent on the PCI Bus selected by the Bus Number. When the Bus Number field is 00 the GMCH decodes the Device Number field. The GMCH is always Device Number 0 for the Host-Hub interface bridge entity. Therefore, when the Bus Number =0 and the Device Number=0-1 the internal GMCH devices are selected. For Bus Numbers resulting in Hub interface Configuration cycles, the GMCH propagates the device number field as A[15:11].
10:8	**Function Number:** This field is mapped to A[10:8] during Hub interface Configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The GMCH ignores Configuration cycles to its internal Devices if the function number is not equal to 0.
7:2	**Register Number:** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address register. This field is mapped to A[7:2] during Hub interface Configuration cycles.
1:0	**Reserved**

4.6.2 CONFIG_DATA – Configuration Data Register

I/O Address:	0CFCh
Default Value:	00000000h
Access:	Read/Write
Size:	32 bits

CONFIG_DATA is a 32-bit Read/Write window into Configuration Space. The portion of Configuration Space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Figure 3. Configuration Data Register



Bit	Descriptions
31:0	**Configuration Data Window (CDW).** If bit 31 of CONFIG_ADDRESS is 1, then any I/O access to the CONFIG_DATA register will be mapped to Configuration Space using the contents of CONFIG_ADDRESS.

4.7 VGA I/O Mapped Registers

If Native Graphics mode is strapped, and Device #2 is enabled, and Function #0 within Device #2 is enabled for VGA, and IO_EN is set within Function #0 then GMCH claims a set of I/O registers for legacy VGA function. Table 17 lists direct CPU Access registers and Table 18 lists registers that are Index – Data registers that are used to access Internal VGA registers.

Table 17. VGA I/O Mapped Register List

Name	Function	Read @	Write @
ST00	VGA Input Status Register 0	3C2h	–
ST01	VGA Input Status Register 1	3BAh/3Dah	–
FCR	VGA Feature Control Register	3CAh	3BAh/3DAh
MSR	VGA Miscellaneous Status/Output Register	3CCh	3C2h

Table 18. Index – Data Registers

Name	Function	Index IO	Data IO
SRX	Sequencer Registers	3C4	3C5
GRX	Graphics Controller Registers	3CE	3CF
ARX	Attribute Control Registers	3C0	3C0: Write 3C1: Read
DACMASK	Pixel Data Mask Register	--	3C6h
DACSTATE	DAC State Register	--	3C7 Read Only
DACRX	Palette Read Index Register	3C7 Write Only	--
DACWX	Palette Write Index Register	3C8 Write Only	
DACDATA	Palette Data Register	3C9	
CRX	CRT Registers	3B4/3D4 (MDA/CGA)	3B5/3D5 (MDA/CGA)

4.8 Intel 854 GMCH Host-Hub Interface Bridge Device Registers (Device #0, Function #0)

Table 5 summarizes the configuration space for Device #0, Function#0.

Table 19. GMCH Configuration Space - Device #0, Function#0

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID	00	01	8086h	RO
Device Identification	DID	02	03	358Ch	RO
PCI Command	PCICMD	04	05	0006h	RO,R/W
PCI Status	PCISTS	06	07	0090h	RO,R/WC
Revision Identification	RID	08	08	02h	RO
Sub-Class Code	SUBC	0A	0A	00h	RO
Base Class Code	BCC	0B	0B	06h	RO
Header Type	HDR	0E	0E	80h	RO
Subsystem Vendor Identification	SVID	2C	2D	0000h	R/WO
Subsystem Identification	SID	2E	2F	0000h	R/WO
Capabilities Pointer	CAPPTR	34	34	40h	RO
Capability Identification	CAPID	40	44	84_A105_0009h	RO
GMCH Misc. Control	GMC	50	51	0000h	R/W
GMCH Graphics Control	GGC	52	53	0030h	R/W
Device and Function Control	DAFC	54	55	0000h	R/W
Fixed Dram Hole Control	FDHC	58	58	00h	R/W
Programmable Attribute Map	PAM (6:0)	59	5F	00h Each	R/W
System Management RAM Control	SMRAM	60	60	02h	R/W/L
Extended System Management RAM Control	ESMRAMC	61	61	38h	R/W/L
Error Status	ERRSTS	62	63	0000h	R/WC
Error Command	ERRCMD	64	65	0000h	R/W
SMI Command	SMICMD	66	66	00h	R/W
SCI Command	SCICMD	67	67	00h	R/W
Secondary Host Interface Control Register	SHIC	74	77	00006010h	RO, R/W

Aperture Translation Table Base	ATTBASE	B8	BB	00000000h	RO, R/W
Host Error Control/Status/ Obs	HEM	F0	F3	00000000h	RO, R/W

4.8.1 VID – Vendor Identification Register

Address Offset:	00-01h
Default Value:	8086h
Access:	Read only
Size:	16 bits

The VID Register contains the vendor identification number. This 16-bit register, combined with the Device Identification Register, uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Descriptions
15:0	**Vendor Identification (VID):** This register field contains the PCI standard identification for Intel.

4.8.2 DID – Device Identification Register

Address Offset:	02-03h
Default Value:	358Ch
Access:	Read only
Size:	16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Descriptions
15:0	**Device Identification (DID):** This is a 16-bit value assigned to the GMCH Host-Hub interface bridge, Device #0.

4.8.3 PCICMD – PCI Command Register

Address Offset:	04-05h
Default Value:	0006h
Access:	Read only, Read/Write
Size:	16 bits

Since GMCH Device #0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Descriptions
15:10	**Reserved**
9	**Fast Back-to-Back Enable (FB2B):** This bit controls whether or not the master can do fast back-to-back Write. Since Device #0 is strictly a target, this bit is not implemented and is hardwired to 0. Writes to this bit position have no affect.
8	**SERR Enable (SERRE):** This bit is a global enable bit for Device #0 SERR messaging. The GMCH does not have an SERR# signal, but communicates the SERR# condition by sending an SERR message to the ICH4-M. 1 = Enable. GMCH is enabled to generate SERR messages over Hub interface for specific Device #0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS and PCISTS registers. 0 = SERR message is not generated by the GMCH for Device #0. **NOTE**: This bit only controls SERR messaging for the Device #0. Device #1 has its own SERRE bit to control error reporting for error conditions occurring on Device #1. The two control bits are used in a logical OR manner to enable the SERR Hub interface message mechanism.
7	**Address/Data Stepping Enable (ADSTEP):** Address/data stepping is not implemented in the GMCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	**Parity Error Enable (PERRE):** PERR# is not implemented by GMCH and this bit is hardwired to 0. Writes to this bit position have no effect.
5	**VGA Palette Snoop Enable (VGASNOOP):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	**Memory Write and Invalidate Enable (MWIE):** The GMCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3	**Special Cycle Enable (SCE):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	**Bus Master Enable (BME):** The GMCH is always enabled as a master on HI. This bit is hardwired to a 1. Writes to this bit position have no effect.
1	**Memory Access Enable (MAE):** The GMCH always allows access to main system memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	**I/O Access Enable (IOAE):** This bit is not implemented in the GMCH and is hardwired to a 0. Writes to this bit position have no effect.

4.8.4 PCI Status Register

Address Offset:	06-07h
Default Value:	0090h
Access:	Read only, Read/WriteClear
Size:	16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device #0's PCI Interface. Bit 14 is Read/Write Clear. All other bits are Read Only. Since GMCH Device #0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Descriptions
15	**Detected Parity Error (DPE):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
14	**Signaled System Error (SSE):** R/WC. This bit is set to 1 when GMCH Device #0 generates an SERR message over HI for any enabled Device #0 error condition. Device #0 error conditions are enabled in the PCICMD and ERRCMD registers. Device #0 error flags are read/reset from the PCISTS or ERRSTS registers. Software sets SSE to 0 by writing a 1 to this bit.
13	**Received Master Abort Status (RMAS):** R/WC. This bit is set when the GMCH generates a HI request that receives a Master Abort completion packet or Master Abort Special Cycle. Software clears this bit by writing a 1 to it.
12	**Received Target Abort Status (RTAS):** R/WC. This bit is set when the GMCH generates a HI request that receives a Target Abort completion packet or Target Abort Special Cycle. Software clears this bit by writing a 1 to it. If bit 6 in the ERRCMD is set to a one and an Serr# special cycle is generated on the HI bus.
11	**Signaled Target Abort Status (STAS):** The GMCH will not generate a Target Abort HI completion packet or Special Cycle. This bit is not implemented in the GMCH and is hardwired to a 0. Writes to this bit position have no effect.
10:9	**DEVSEL Timing (DEVT):** These bits are hardwired to “00”. Writes to these bit positions have no affect. Device #0 does not physically connect to PCI_A. These bits are set to “00” (fast decode) so that the GMCH does not limit optimum DEVSEL timing for PCI_A.
8	**Master Data Parity Error Detected (DPD):** PERR signaling and messaging are not implemented by the GMCH therefore this bit is hardwired to 0. Writes to this bit position have no effect.
7	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1. Writes to these bit positions have no effect. Device #0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the GMCH does not limit the optimum setting for PCI_A.
6:5	**Reserved**
4	**Capability List (CLIST):** This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h.
3:0	**Reserved**

4.8.5 RID – Register Identification

Address Offset:	08h
Default Value:	02h
Access:	Read only
Size:	8 bits

This register contains the revision number of the GMCH Device #0. These bits are read only and writes to this register have no effect.

Bit	Descriptions
7:0	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the GMCH Device #0.

4.8.6 SUBC – Sub Class Code Register

Address Offset:	0Ah
Default Value:	00h
Access:	Read only
Size:	8 bits

This register contains the Sub-Class Code for the GMCH Device #0. This code is 00h indicating a Host Bridge device.

Bit	Descriptions
7:0	**Sub-Class Code (SUBC)**: This is an 8-bit value that indicates the category of Bridge into which the GMCH falls. The code is 00h indicating a Host Bridge.

4.8.7 BCC – Base Class Code Register

Address Offset:	0Bh
Default Value:	06h
Access:	Read only
Size:	8 bits

This register contains the Base Class code of the GMCH Device #0. This code is 06h indicating a Bridge device.

Bit	Descriptions
7:0	**Base Class Code (BASEC):** This is an 8-bit value that indicates the Base Class Code for the GMCH. This code has the value 06h, indicating a Bridge device.

4.8.8 HDR – Header Type Register

Address Offset:	0Eh
Default Value:	80h
Access:	Read only
Size:	8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	**PCI Header (HDR):** This field always returns 80 to indicate that Device #0 is a multifunction device. If Functions other than 0 are disabled, this field returns a 00 to indicate that the GMCH is a single function device with standard header layout. Writes to this location have no effect.

4.8.9 SVID – Subsystem Vendor Identification Register

Address Offset:	2C-2Dh
Default Value:	0000h
Access:	Read/Write Once
Size:	16 bits

This value is used to identify the vendor of the subsystem.

Bit	Descriptions
15:0	**Subsystem Vendor ID (SUBVID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes Read Only.

4.8.10 SID – Subsystem Identification Register

Address Offset:	2E-2Fh
Default Value:	0000h
Access:	Read/Write Once
Size:	16 bits

This value is used to identify a particular subsystem.

Bit	Descriptions
15:0	**Subsystem ID (SUBID)**: This field should be programmed during BIOS initialization. After it has been written once, it becomes Read Only.

4.8.11 CAPPTR – Capabilities Pointer Register

Address Offset:	34h
Default Value:	40h
Access:	Read Only
Size:	8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Descriptions
7:0	**Pointer to the offset of the first capability ID register block**: In this case the first capability is the Product-Specific Capability, which is located at offset 40h.

4.8.12 CAPID – Capabilities Identification Register (Device #0)

Address Offset:	40-44h
Default Value:	chipset independent
Access:	Read Only
Size:	40 bits

The Capability Identification Register uniquely identifies chipset capabilities as defined in the table below. The bits in this register are intended to define a capability ceiling for each feature, not a capability select. The capability selection for each feature is implemented elsewhere. The mechanism to select the capability for each feature must comprehend these Capability registers and not allow a selected setting above the ceiling specified in these registers. The BIOS must read this register to identify the part and comprehend the capabilities specified within when configuring the effected portions of the GMCH.

The default setting, in most cases, allows the maximum capability. Exceptions are noted in the individual bits. This register is Read Only. Writes to this register have no effect.

Bit	Descriptions
39:37	**Capability ID [2:0]**: 000: Intel® 82854 GMCH 001-111: Reserved
36:28	**Reserved**
27:24	**CAPREG Version:** This field has the value 0001b to identify the first revision of the CAPREG definition.
23:16	**Cap_length:** This field has the value 05h indicating the structure length.
15:0	**Reserved**

4.8.13 GMC – GMCH Miscellaneous Control Register (Device #0)

Address Offset: 50-51h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

Bit	Descriptions
15:10	**Reserved**
9	**Reserved**
8	**RRBAR Access Enable—R/W**: 1: Enables the RRBAR space. 0: Disable
7:1	**Reserved**
0	**MDA Present (MDAP)—R/W**: This bit should not be set when the VGA Enable bit is not set. If the VGA enable bit is set, then accesses to IO address range x3BCh–x3BFh are forwarded to Hub interface. If the VGA enable bit is not set then accesses to IO address range x3BCh–x3BFh are treated just like any other IO accesses. MDA resources are defined as the following: Memory: 0B0000h – 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to Hub interface even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: **VGA** **MDA Behavior** 0 0 All References to MDA and VGA go to Hub interface (Default) 0 1 Reserved 1 0 All References to VGA go to PCI. MDA-only references (I/O address 3BF and aliases will go to Hub interface. 1 1 VGA References go to PCI; MDA References go to Hub interface

4.8.14 GGC – GMCH Graphics Control Register (Device #0)

Address Offset:	52-53h
Default Value:	0030h
Access:	Read/Write
Size:	16 bits

Bit	Descriptions
15:7	**Reserved**
6:4	**Graphics Mode Select (GMS):** This field is used to select the amount of Main system memory that is pre-allocated to support the Internal Graphics Device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that system memory is pre-allocated only when Internal Graphics is enabled. 000: No system memory pre-allocated. Device #2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within Device #2 Function #0 Class Code register is 80. 001: DVMT (UMA) mode, 1 MB of system memory pre-allocated for frame buffer. 010: DVMT (UMA) mode, 4 MB of system memory pre-allocated for frame buffer. 011: DVMT (UMA) mode, 8 MB of system memory pre-allocated for frame buffer. 100: DVMT (UMA) mode, 16 MB of system memory pre-allocated for frame buffer. 101: DVMT (UMA) mode, 32 MB of system memory pre-allocated for frame buffer. All other combinations reserved.
3	**Reserved**
2	**Device #2 Function #1 Enable/Disable**: 1: Disable Function #1 within Device #2. 0: Enable Function #1 within Device #2.
1	**IGD VGA Disable (IVD):** VGA can only be enabled in Naytive Graphics Mode. If strapped in other mode, this bit should always set to 1. 1: Disable. Device #2 (IGD) does not claim VGA Memory and I/O Mem cycles, and the Sub-Class Code field within Device #2 Function #0 Class Code register is 80. 0: Enable. Device #2 (IGD) claims VGA Memory and I/O cycles, the Sub-Class Code within Device #2 Class Code register is 00.
0	**Reserved**

4.8.15 DAFC – Device and Function Control Register (Device #0)

Address Offset:	54-55h
Default Value:	0000h
Access:	Read/Write
Size:	16 bits

This 16-bit register controls the visibility of devices and functions within the GMCH to configuration software.

Bit	Description
15:8	**Reserved**
7	**Device #2 Disable**: 1: Disabled. 0: Enabled.
6:3	**Reserved**
2	**Device #0 Function #3 Disable**: 1: Disable Function #3 registers within Device #0 and all associated DDR SDRAM and I/O ranges. 0: Enable Function #3 within Device #0.
1	**Reserved**
0	**Device #0 Function #1 Disable**: 1: Disable Function #1 within Device #0. 0: Enable Function #1 within Device #0.

4.8.16 FDHC – Fixed DRAM Hold Control Register (Device #0)

Address Offset:	58h
Default Value:	00h
Access:	Read/Write
Size:	8 bits

This 8-bit register controls a single fixed DDR SDRAM hole: 15-16 MB.

Bit	Description
7	**Hole Enable (HEN):** This field enables a memory hole in DDR SDRAM space. Host cycles matching an enabled hole are passed onto ICH4-M through Hub interface. The GMCH will ignore Hub interface cycles matching an enabled hole. **NOTE**: A selected hole is not re-mapped. 0: None 1: 15 MB–16 MB (1MBs)
6:0	Reserved

4.8.17 PAM(6:0) – Programmable Attribute Map Register (Device #0)

Address Offset:	59-5Fh
Default Value:	00h Each
Access:	Read/Write
Size:	4 bits/register, 14 registers

The GMCH allows programmable DDR SDRAM attributes on 13 Legacy system memory segments of various sizes in the 640 kB -1 MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the P6 processor. Two bits are used to specify system memory attributes for each system memory segment. These bits apply to both Host and Hub interface initiator accesses to the PAM areas. These attributes are:

- **RE - Read Enable**. When RE = 1, the CPU Read accesses to the corresponding system memory segment are claimed by the GMCH and directed to main system memory. Conversely, when RE = 0, the Host Read accesses are directed to PCI0.
- **WE - Write Enable**. When WE = 1, the Host Write accesses to the corresponding system memory segment are claimed by the GMCH and directed to main system memory. Conversely, when WE = 0, the Host Write accesses are directed to PCI0.

The RE and WE attributes permit a system memory segment to be Read Only, Write Only, Read/Write, or Disabled. For example, if a system memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM register controls two regions, typically 16 kB in size. Each of these regions has a 4-bit field. The 4 bits that control each region have the same encoding and are defined in the following table.

Table 20. Attribute Bit Assignment

Bits [7, 3] Reserved	Bits [6, 2] Reserved	Bits [5, 1] WE	Bits [4, 0] RE	Description
X	X	0	0	**Disabled**. DDR SDRAM is disabled and all accesses are directed to Hub interface. The GMCH does not respond as a Hub interface target for any Read or Write access to this area.
X	X	0	1	**Read Only**. Reads are forwarded to DDR SDRAM and Writes are forwarded to Hub interface for termination. This Write protects the corresponding DDR SDRAM segment. The GMCH will respond as a Hub interface target for Read accesses but not for any Write accesses.
X	X	1	0	**Write Only**. Writes are forwarded to DDR SDRAM and Reads are forwarded to the Hub interface for termination. The GMCH will respond as a Hub interface target for Write accesses but not for any Read accesses.
X	X	1	1	**Read/Write**. This is the normal operating mode of main system memory. Both Read and Write cycles from the host are claimed by the GMCH and forwarded to DDR SDRAM. The GMCH will respond as a Hub interface target for both Read and Write accesses.

As an example, consider a BIOS that is implemented on the Expansion bus. During the initialization process, the BIOS can be shadowed in main system memory to increase the system performance. When BIOS is shadowed in main system memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to Write Only. The BIOS is shadowed by first doing a Read of that address. This Read is forwarded to the Expansion bus. The Host then does a Write of the same address, which is directed to main system memory. After the BIOS is shadowed, the attributes for that system memory area are set to Read Only so that all Writes are forwarded to the Expansion bus. Figure 4 and Table 21 show the PAM registers and the associated attribute bits.

Figure 4. PAM Registers

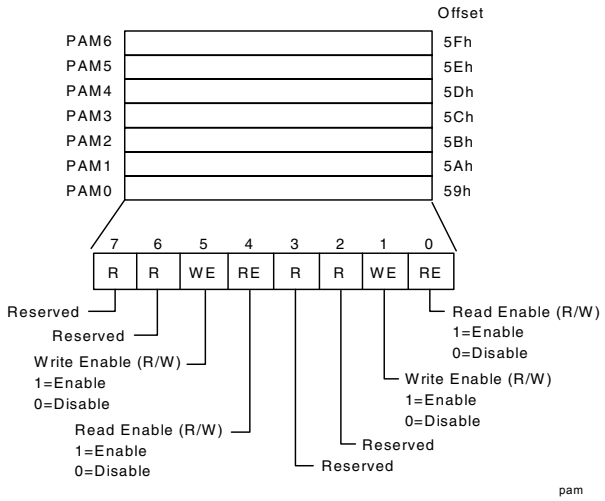


Table 21. PAM Registers and Associated System Memory Segments

PAM Reg	Attribute Bits			System Memory Segment		Comments	Offset
PAM0[3:0]	Reserved						59h
PAM0[7:4]	R	R	WE	RE	0F0000h–0FFFFFh	BIOS Area	59h
PAM1[3:0]	R	R	WE	RE	0C0000h–0C3FFFh	ISA Add-on BIOS	5Ah
PAM1[7:4]	R	R	WE	RE	0C4000h–0C7FFFh	ISA Add-on BIOS	5Ah
PAM2[3:0]	R	R	WE	RE	0C8000h–0CBFFFh	ISA Add-on BIOS	5Bh
PAM2[7:4]	R	R	WE	RE	0CC000h–0CFFFFh	ISA Add-on BIOS	5Bh
PAM3[3:0]	R	R	WE	RE	0D0000h–0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	R	WE	RE	0D4000h–0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	R	WE	RE	0D8000h–0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	R	WE	RE	0DC000h–0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	R	WE	RE	0E0000h–0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	R	WE	RE	0E4000h–0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	R	WE	RE	0E8000h–0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	R	WE	RE	0EC000h–0EFFFFh	BIOS Extension	5Fh

For details on overall system address mapping scheme see the Address Decoding section of this document.

DOS Application Area (00000h-9FFFh)

The DOS area is 640 kB in size and it is further divided into two parts. The 512-kB area at 0 to 7FFFFh is always mapped to the main system memory controlled by the GMCH, while the 128-kB address range from 080000 to 09FFFFh can be mapped to PCI0 or to main DDR SDRAM. By default this range is mapped to main system memory and can be declared as a main system memory hole (accesses forwarded to PCI0) via GMCH's FDHC Configuration register.

Video Buffer Area (A0000h-BFFFFh)

Attribute Bits do not control this 128-kB area. The Host-initiated cycles in this region are always forwarded to either PCI0 or PCI2 unless this range is accessed in SMM mode. ***Routing of accesses is controlled by the Legacy VGA Control Mechanism of the "Virtual" PCI-PCI Bridge Device embedded within the GMCH***.

This area can be programmed as SMM area via the SMRAM register. When the GMCH is strapped in other mode, or when used as an SMM space, this range can not be accessed from the Hub interface.

Expansion Area (C0000h-DFFFFh)

This 128-kB area is divided into eight 16-kB segments that can be assigned with different attributes via PAM Control register as defined in Figure 4 and Table 21.

Extended System BIOS Area (E0000h-EFFFFh)

This 64-kB area is divided into four 16-kB segments that can be assigned with different attributes via PAM Control register as defined in Figure 4 and Table 21.

System BIOS Area (F0000h-FFFFFh)

This area is a single 64-kB segment that can be assigned with different attributes via PAM Control register as defined in Figure 4 and Table 21.

4.8.18 SMRAM – System Management RAM Control Register (Device #0)

Address Offset:	60h
Default Value:	02h
Access:	Read/Write/Lock, Read Only
Size:	8 bits

The SMRAM register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock Bits function only when G_SMRAME Bit is set to a 1. Also, the Open Bit must be Reset before the LOCK Bit is set.

Bit	Description
7	**Reserved**
6	**SMM Space Open (D_OPEN):** When D_OPEN=1 and D_LCK=0, the SMM space DDR SDRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. When D_LCK is set to a 1, D_OPEN is Reset to 0 and becomes Read Only.
5	**SMM Space Closed (D_CLS):** When D_CLS = 1 SMM Space, DDR SDRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DDR SDRAM. This will allow SMM software to reference “through” SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. D_CLS applies to all SMM spaces (Cseg, Hseg, and Tseg).
4	**SMM Space Locked (D_LCK):** When D_LCK is set to 1, then D_OPEN is Reset to 0 and D_LCK, D_OPEN, G_SMRAME, C_BASE_SEG, GMS, DRB, DRA, H_SMRAM_EN, TSEG_SZ and TSEG_EN become Read Only. D_LCK can be set to 1 via a normal Configuration Space Write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to “lock down” SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	**Global SMRAM Enable (G_SMRAME):** If set to a 1, then Compatible SMRAM functions is enabled, providing 128 kB of DDR SDRAM accessible at the A0000h address while in SMM (ADS# with SMM decode). To enable Extended SMRAM function this bit must be set to 1, refer to the section on SMM for more details. Once D_LCK is set, this bit becomes Read Only.
2:0	**Compatible SMM Space Base Segment (C_BASE_SEG)—RO:** This field indicates the location of SMM space. “SMM DRAM” is not remapped. It is simply “made visible” if the conditions are right to access SMM space, otherwise the access is forwarded to Hub interface. C_BASE_SEG is hardwired to 010 to indicate that the GMCH supports the SMM space at A0000h–BFFFFh.

4.8.19 ESMRAMC – Extended System Management RAM Control (Device #0)

Address Offset:	61h
Default Value:	38h
Access:	Read/Write/Lock
Size:	8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM Space. The Extended SMRAM (E_SMRAM) Memory provides a Write-Back cacheable SMRAM Memory Space that is above 1 MB.

Bit	Description
7	**H_SMRAM_EN (H_SMRAME):** Controls the SMM Memory Space location (that is, above 1 MB or below 1 MB). When G_SMRAME is 1 and H_SMRAME this bit is set to 1, the high SMRAM Memory Space is enabled. SMRAM accesses from 0FEDA0000h to 0FEDBFFFFh are remapped to DDR SDRAM address 000A0000h to 000BFFFFh. Once D_LCK is set, this bit becomes Read Only.
6	**E_SMRAM_ERR (E_SMERR):** This bit is set when CPU accesses the defined DDR SDRAM ranges in Extended SMRAM (High system memory and T-segment) while not in SMM Space. It is software's responsibility to clear this bit. The software must Write a 1 to this bit to clear it.
5	**SMRAM_Cache (SM_CACHE):** GMCH forces this bit to 1.
4	**SMRAM_L1_EN (SM_L1):** GMCH forces this bit to 1.
3	**SMRAM_L2_EN (SM_L2):** GMCH forces this bit to 1.
2:1	**Reserved**
0	**TSEG_EN (T_EN):** Enabling of SMRAM Memory (TSEG, 1 Mbytes of additional SMRAM Memory) for Extended SMRAM Space only. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Once D_LCK is set, this bit becomes Read Only.

4.8.20 ERRSTS – Error Status Register (Device #0)

Address Offset:	62-63h
Default Value:	0000h
Access:	Read/Write Clear
Size:	16 bits

This register is used to report various error conditions via Hub Interface Special cycles. An SERR, SMI, or SCI Error Hub Interface Special cycle may be generated on a zero to one transition of any of these flags when enabled in the PCICMD/ERRCMD, SMICMD, or SCICMD registers respectively.

Bit	Description
15:14	**Reserved**
13	**FSB Strobe Glitch Detected (FSBAGL):** When this bit is set to 1 the GMCH has detected a glitch on one of the FSB strobes. Writing a 1 to it clears this bit.
12	**GMCH Software Generated Event for SMI**: 1: This indicates the source of the SMI was a Device #2 Software Event. 0: Software must Write a 1 to clear this bit.
11	**GMCH Thermal Sensor Event for SMI/SCI/SERR**: 1: Indicates that a GMCH Thermal Sensor trip has occurred and an SMI, SCI or SERR has been generated. Note that the status bit is set only if a message is sent based on Thermal event enables in Error Command, SMI Command and SCI Command registers. Note that a Trip Point can generate one of SMI, SCI or SERR interrupts (two or more per event is illegal). Multiple Trip Points can generate the same interrupt. If software chooses this mode, then subsequent Trips may be lost. 0: Software must Write a 1 to clear this status bit. If this bit is set, then an interrupt message will not be sent on a new Thermal Sensor event.
10	**Reserved**
9	**LOCK to non-DDR SDRAM Memory Flag (LCKF)—R/WC**: 1: Indicates that a CPU initiated LOCK cycle targeting non-DDR SDRAM Memory Space occurred. 0: Software must Write a 1 to clear this status bit
8	**Received Refresh Timeout—R/WC**: 1: This bit is set when 1024 memory core refresh are Queued up. 0: Software must Write a 1 to clear this status bit.
7	**DRAM Throttle Flag (DTF)—R/WC**: 1: Indicates that the DDR SDRAM Throttling condition occurred. 0: Software must Write a 1 to clear this status bit.
6	**Reserved**
5	**Received Unimplemented Special Cycle Hub Interface Completion Packet FLAG (UNSC)—R/WC**: 1: Indicates that the GMCH initiated a Hub interface request that was terminated with an Unimplemented Special Cycle completion packet. 0: Software must Write a 1 to clear this status bit.
4:0	**Reserved**

4.8.21 ERRCMD – Error Command Register (Device #0)

Address Offset:	64-65h
Default Value:	0000h
Access:	Read/Write Clear
Size:	16 bits

This register enables various errors to generate a SERR Hub Interface Special cycle. Since the GMCH does not have a SERR# signal, SERR messages are passed from the GMCH to the ICH4-M over Hub interface. **The actual generation of the SERR message is globally enabled for Device #0 via the PCI Command register**.

Note: An error can generate one and only one Hub Interface Error Special cycle. It is software's responsibility to make sure that when an SERR error message is enabled for an error condition, SMI and SCI error messages are disabled for that same error condition.

Bit	Description
15:14	**Reserved**
13	**SERR on FSB Strobe Glitch:** When this bit is asserted, the GMCH will generate a HI SERR message when a glitch is detected on one of the FSB strobes.
12	**Reserved**
11	**SERR on GMCH Thermal Sensor Event**: 1: The GMCH generates a SERR Hub Interface Special cycle on a Thermal Sensor Trip that requires an SERR. The SERR must not be enabled at the same time as the SMI/SCI for a Thermal Sensor Trip event. 0: Software must write a 1 to clear this status bit.
10	**Reserved**
9	**SERR on LOCK to non-DDR SDRAM Memory**: 1: The GMCH generates an SERR Hub Interface Special cycle when a CPU initiated LOCK transaction targeting non-DDR SDRAM Memory Space occurs. 0: Reporting of this condition is disabled.
8	**SERR on DDR SDRAM Refresh timeout**: 1: The GMCH generates an SERR Hub Interface Special cycle when a DDR SDRAM Refresh timeout occurs. 0: Reporting of this condition is disabled.
7	**SERR on DDR SDRAM Throttle Condition**: 1: The GMCH generates an SERR Hub Interface Special cycle when a DDR SDRAM Read or Write Throttle condition occurs. 0: Reporting of this condition is disabled.
6	**SERR on Receiving Target Abort on Hub Interface**: 1: The GMCH generates an SERR Hub Interface Special cycle when a GMCH originated Hub interface cycle is terminated with a Target Abort. 0: Reporting of this condition is disabled.

5	**SERR on Receiving Unimplemented Special Cycle Hub Interface Completion Packet**: 1: The GMCH generates an SERR Hub Interface Special cycle when a GMCH initiated Hub interface request is terminated with a Unimplemented Special cycle completion packet. 0: Reporting of this condition is disabled.
4:2	**Reserved**
1	**SERR on Multiple-bit ECC Error**: 0: This system does not support ECC, this field must be set to 0.
0	**SERR on Single-bit ECC Error**: 0: This system does not support ECC, this field must be set to 0.

4.8.22 SMICMD – SMI Error Command Register (Device #0)

Address Offset:	66h
Default Value:	00h
Access:	Read/Write
Size:	8 bits

This register enables various errors to generate an SMI Hub Interface Special cycle. When an Error Flag is set in the ERRSTS register, it can generate a SERR, SMI, or SCI Hub Interface Special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers respectively.

Note: An error can generate one and only one Hub Interface Error Special cycle. It is software's responsibility to make sure that when an SMI Error Message is enabled for an error condition, SERR, and SCI Error Messages are disabled for that same error condition.

Bit	Description
7:4	**Reserved**
3	**SMI on GMCH Thermal Sensor Trip**: 1: An SMI Hub Interface Special cycle is generated by GMCH when the Thermal Sensor Trip requires an SMI. A Thermal Sensor Trip Point cannot generate more than one special cycle.
2	**Reserved**
1	**SMI on Multiple-bit ECC Error**: 0: This system does not support ECC, this field must be set to 0.
0	**SMI on Single-bit ECC Error**: 0: This system does not support ECC, this field must be set to 0.

4.8.23 SCICMD – SCI Error Command Register (Device #0)

Address Offset:	67h
Default Value:	00h
Access:	Read/Write
Size:	8 bits

This register enables various errors to generate a SCI Hub Interface Special cycle. When an Error Flag is set in the ERRSTS register, it can generate a SERR, SMI, or SCI Hub Interface Special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers respectively.

Note: An error can generate one and only one Hub Interface Error Special cycle. It is software's responsibility to make sure that when an SCI error message is enabled for an error condition, SERR and SMI Error Messages are disabled for that same error condition.

Bit	Description
7:4	**Reserved**
3	**SCI on GMCH Thermal Sensor Trip**: 1: An SCI Hub Interface Special cycle is generated by GMCH when the Thermal Sensor Trip requires an SCI. A Thermal Sensor Trip Point cannot generate more than one special cycle.
2	**Reserved**
1	**SCI on Multiple-bit ECC Error**: 0: This system does not support ECC, this field must be set to 0.
0	**SCI on Single-bit ECC Error**: 0: This system does not support ECC, this field must be set to 0.

4.8.24 SHIC – Secondary Host Interface Control Register (Device #0)

Address Offset: 74-77h
Default Value: 00006010h
Access: Read Only, Read/Write
Size: 32 bits

Bit	Descriptions
31	**Reserved**
30	**BREQ0# Control of FSB Address and Control bus power management**: 0: Disable FSB address and control bus power management. 1: Eisable FSB address and control bus power management.
29:28	**Reserved**
27	**On Die Termination (ODT) Gating Disable**: 0: Enable. 1: Disable.
26:7	**Reserved**
6	**FSB Data Bus Power Management Control**: 0: FSB Data Bus Power Management disabled (Default). 1: FSB Data Bus Power Management enabled
5	**Reserved**
4:3	**DPWR# Control**. 00: DPWR# pin is always asserted. 10: DPWR# pin is asserted at least 2 clocks before read data is returned to the processor on the FSB (2 clocks before DRDY# asserted). This is default setting. 01: DPWR# is always de-asserted. 11: Reserved
2	**C2 state GMCH FSB Interface Power Management Control**: 0: Power Management Disabled in C2 state 1: Power Management Enabled in C2 state
1	**Reserved**.
0	**Reserved**

4.8.25 HEM – Host Error Control, Status, and Observation (Device #0)

Address Offset: F0-F3h
Default Value: 00000000h
Access: Read Only, Read/Write
Size: 32 bits

Bit	Description
31	**Detected HADSTB1# Glitch (ASTB1GL):** This bit is set when the GMCH has detected a glitch on address strobe HADSTB1#. Software must write a 1 to clear this status bit.
30	**Detected HADSTB0# Glitch (ASTB0GL):** This bit is set when the GMCH has detected a glitch on address strobe HADSTB0#. Software must write a 1 to clear this status bit.
29	**Detected HDSTB3# Glitch (DSTB3GL):** This bit is set when the GMCH has detected a glitch on data strobe pair HDSTB3#. Software must write a 1 to clear this status bit.
28	**Detected HDSTB2# Glitch (DSTB2GL):** This bit is set when the GMCH has detected a glitch on data strobe pair HDSTB2#. Software must write a 1 to clear this status bit.
27	**Detected HDSTB1# Glitch (DSTB1GL):** This bit is set when the GMCH has detected a glitch on data strobe pair HDSTB1#. Software must write a 1 to clear this status bit.

4.9 Intel 854 GMCH Main Memory Control, Memory I/O Control Registers (Device #0, Function #1)

The following table shows the GMCH Configuration Space for Device #0, Function #1. See "Nomenclature for Access Attributes" on page 42 for access nomenclature.

Table 22. Host-Hub I/F Bridge/System Memory Controller Configuration Space (Device #0, Function#1)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID	00	01	8086h	RO
Device Identification	DID	02	03	358Ch	RO
PCI Command	PCICMD	04	05	0006h	RO,R/W
PCI Status	PCISTS	06	07	0080h	RO,R/WC
Revision Identification	RID	08	08	02h	RO
Sub-Class Code	SUBC	0A	0A	80h	RO
Base Class Code	BCC	0B	0B	08h	RO
Header Type	HDR	0E	0E	80h	RO
Subsystem Vendor Identification	SVID	2C	2D	0000h	R/WO
Subsystem Identification	SID	2E	2F	0000h	R/WO
Capabilities Pointer	CAPPTR	34	34	00h	RO
DRAM Row 0-3 Boundary	DRB	40	43	00000000h	RW
DRAM Row 0-3 Attribute	DRA	50	51	7777h	RW
DRAM Timing	DRT	60	63	18004425h	RW
DRAM Controller Power Management Control	PWRMG	68	6B	00000000h	R/W
Dram Controller Mode	DRC	70	73	00000081h	R/W
DRAM Throttle Control	DTC	A0	A3	00000000h	R/W/L

4.9.1 VID – Vendor Identification Register

Address Offset:	00-01h
Default Value:	8086h
Access:	Read Only
Size:	16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Descriptions
15:0	**Vendor Identification (VID):** This register field contains the PCI standard identification for Intel.

4.9.2 DID – Device Identification Register

Address Offset:	02-03h
Default Value:	358Ch
Access:	Read Only
Size:	16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Descriptions
15:0	**Device Identification Number (DID)**: This is a 16-bit value assigned to the GMCH Host- HI Bridge Function #1 (358Ch).

4.9.3 PCICMD – PCI Command Register

Address Offset:	04-05h
Default Value:	0006h
Access:	Read Only, Read/Write
Size:	16 bits

Since Intel chipset Device #0 does not physically reside on PCI_A, many of the bits are not implemented.

Bit	Descriptions
15:10	**Reserved**
9	**Fast Back-to-Back Enable (FB2B):** This bit controls whether or not the master can do fast back-to-back Write. Since Device #0 is strictly a target, this bit is not implemented and is hardwired to 0. Writes to this bit position have no affect.
8	**SERR Enable (SERRE):** SERR# is not implemented by Function #1 of Device #0 of the GMCH and this bit is hardwired to 0. Writes to this bit position have no effect.
7	**Address/Data Stepping Enable (ADSTEP):** Address/data stepping is not implemented in the GMCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	**Parity Error Enable (PERRE):** PERR# is not implemented by GMCH and this bit is hardwired to 0. Writes to this bit position have no effect.
5	**VGA Palette Snoop Enable (VGASNOOP):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	**Memory Write and Invalidate Enable (MWIE):** The GMCH will never issue Memory Write and Invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3	**Special Cycle Enable (SCE):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	**Bus Master Enable (BME):** The GMCH is always enabled as a master on HI. This bit is hardwired to a 1. Writes to this bit position have no effect.
1	**Memory Access Enable (MAE):** The GMCH always allows access to main system memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	**I/O Access Enable (IOAE):** This bit is not implemented in the GMCH and is hardwired to a 0. Writes to this bit position have no effect.

4.9.4 PCISTS – PCI Status Register

Address Offset:	06-07h
Default Value:	0080h
Access:	Read Only, Read/Write Clear
Size:	16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device #0's PCI Interface. Bit 14 is Read/Write Clear. All other bits are Read Only. Since GMCH Device #0 does not physically reside on PCI_A, many of the bits are not implemented.

Bit	Descriptions
15	**Detected Parity Error (DPE):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
14	**Signaled System Error (SSE):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
13	**Received Master Abort Status (RMAS):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
12	**Received Target Abort Status (RTAS):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
11	**Signaled Target Abort Status (STAS):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
10:9	**DEVSEL Timing (DEVT):** These bits are hardwired to “00”. Writes to these bit positions have no affect. Device #0 does not physically connect to PCI_A. These bits are set to “00” (fast decode) so that the GMCH does not limit optimum DEVSEL timing for PCI_A.
8	**Master Data Parity Error Detected (DPD):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
7	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1. Writes to these bit positions have no effect. Device #0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the GMCH does not limit the optimum setting for PCI_A.
6:5	**Reserved**
4	**Capability List (CLIST):** This bit is hardwired to 0 to indicate to the configuration software that this device/function does not implement new capabilities. Default Value = 0
3:0	**Reserved**

4.9.5 RID – Revision Identification Register

Address Offset:	08h
Default Value:	02h
Access:	Read Only
Size:	8 bits

This register contains the revision number of the Intel® 82854 GMCH Device #0. These bits are Read Only and Writes to this register have no effect.

Bit	Descriptions
7:0	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the GMCH Device #0.

4.9.6 RID – Revision Identification Register

Address Offset:	0Ah
Default Value:	80h
Access:	Read Only
Size:	8 bits

This register contains the Sub-Class code for the Intel® 82854 GMCH Device #0. This code is 80h indicating Other Peripheral device.

Bit	Descriptions
7:0	**Sub-Class Code (SUBC)**: This is an 8-bit value that indicates the category of Peripheral device into which the GMCH Function #1 falls. The code is 80h indicating Other Peripheral device.

4.9.7 BCC – Base Class Code Register

Address Offset:	0Bh
Default Value:	08h
Access:	Read Only
Size:	8 bits

This register contains the Base Class code of the Intel® 82854 GMCH Device #0 Function #1. This code is 08h indicating Other Peripheral device.

Bit	Descriptions
7:0	**Base Class Code (BASEC)**: This is an 8-bit value that indicates the Base Class Code for the GMCH. This code has the value 08h, indicating Other Peripheral device.

4.9.8 HDR – Header Type Register

Address Offset:	0Eh
Default Value:	80h
Access:	Read Only
Size:	8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	**PCI Header (HDR)**: This field always returns 80 to indicate that Device #0 is a multifunction device. Reads and Writes to this location have no effect.

4.9.9 SVID – Subsystem Vendor Identification Register

Address Offset:	2C-2Dh
Default Value:	0000h
Access:	Read/Write Once
Size:	16 bits

This value is used to identify the vendor of the subsystem.

Bit	Descriptions
15:0	**Subsystem Vendor ID (SUBVID)**: This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes Read Only.

4.9.10 SID – Subsystem Identification Register

Address Offset:	2E-2Fh
Default Value:	0000h
Access:	Read/Write Once
Size:	16 bits

This value is used to identify a particular subsystem.

Bit	Descriptions
15:0	**Subsystem ID (SUBID)**: This field should be programmed during BIOS initialization. After it has been Written once, it becomes Read Only.

4.9.11 CAPPTR – Capabilities Pointer Register

Address Offset:	34h
Default Value:	00h
Access:	Read Only
Size:	8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Descriptions
7:0	**Pointer to the offset of the first capability ID register block**: In this case there are no capabilities, therefore these bits are hardwired to 00h to indicate the end of the capability linked list.

4.9.12 DRB – DRAM Row (0:3) Boundary Register (Device #0)

Address Offset:	40-43h
Default Value:	00h each
Access:	Read/Write
Size:	8 bits each

The DDR SDRAM Row Boundary Register defines the upper boundary address of each DDR SDRAM row with a granularity of 32 MB. Each row has its own single-byte DRB register. For example, a value of 1 in DRB0 indicates that 32 MB of DDR SDRAM has been populated in the first row. Since the GMCH supports a total of four rows of system memory, DRB0-3 are used. The registers from 44h-4Fh are Reserved for DRBs 4-15.

Row0: 40h
Row1: 41h
Row2: 42h
Row3: 43h

44h to 4Fh is reserved.

DRB0 = Total system memory in Row0 (in 32-MB increments)
DRB1 = Total system memory in Row0 + Row1 (in 32-MB increments)
DRB2 = Total system memory in Row0 + Row1 + Row2 (in 32-MB increments)
DRB3 = Total system memory in Row0 + Row1 + Row2 + Row3 (in 32-MB increments)

Each Row is represented by a Byte. Each Byte has the following format.

Bit	Descriptions
7:0	**DDR SDRAM Row Boundary Address**: This 8-bit value defines the upper and lower addresses for each DDR SDRAM row. This 8-bit value is compared against a set of address lines to determine the upper address limit of a particular row. Also the minimum system memory supported is 64 MB in 64-Mb granularity; hence bit 0 of this register must be programmed to a zero.

4.9.13 DRA – DRAM Row Attribute Register (Device #0)

Address Offset:	50-51h
Default Value:	77h
Access:	Read/Write
Size:	8 bits

The DDR SDRAM **Row Attribute Register** defines the page sizes to be used when accessing different pairs of Rows. Each Nibble of information in the **DRA** registers describes the page size of a pair of Rows:

Row 0, 1: 50h

Row 2, 3: 51h

52h-5Fh: Reserved.

7	6 ... 4	3	2 ... 0
R	Row attribute for Row1	R	Row Attribute for Row0

7	6 ... 4	3	2 ... 0
R	Row attribute for Row3	R	Row Attribute for Row2

Bit	Description
7	Reserved
6:4	**Row Attribute for odd-numbered Row:** This field defines the page size of the corresponding row. 000: Reserved 001: 4 kB 010: 8 kB 011: 16 kB 111: Not Populated Others: Reserved
3	Reserved
2:0	**Row Attribute for even-numbered Row:** This field defines the page size of the corresponding row. 000: Reserved 001: 4 kB 010: 16 kB 111: Not Populated Others: Reserved

4.9.14 DRT – DRAM Timing Register (Device #0)

Address Offset:	60-63h
Default Value:	18004425h
Access:	Read/Write
Size:	32 bits

This register controls the timing of the DDR SDRAM controller.

Bit	Description
31	**DDR Internal Write to Read Command delay (tWTR)**: The tWTR is a std. DDR SDRAM timing parameter with a value of 1 CK for CL=2 and 2.5. The tWTR is used to time RD command after a WR command (to same Row): 0: tWTR is set to 1 Clock (CK), used for DDR SDRAM CL=2 or 2.5 1: Reserved
30	**DDR Write Recovery time (tWR)**: Write recovery time is a std. DDR timing parameter with the value of 15 ns. It should be set to 2 CK when DDR200 is used. The tWR is used to time PRE command launch after a WR command, when DDR SDRAM components are populated. 0: tWR is set to 2 Clocks (CK) 1: tWR is set to 3 Clocks (CK)
29:28	**Back To Back Write-Read commands spacing (DDR different Rows/Bank):** This field determines the WR-RD command spacing, in terms of common clocks for DDR SDRAM based on the following formula: DQSS + 0.5xBL + TA (WR-RD) – CL DQSS: is time from Write command to data and is always 1 CK BL: is Burst Length and can be set to 4. TA (WR-RD): is required DQ turn-around, can be set to 1 or 2 CK CL: is CAS Latency, can be set to 2 or 2.5 **Examples of usage**: For BL=4, with single DQ turn-around and CL=2, this field must be set to 2 CK (1+2+1-2) **Encoding** **CK between WR and RD commands** 00: 4 01: 3 10: 2 11: Reserved

27:26	**Back To Back Read-Write commands spacing (DDR, same or different Rows/Bank):** This field determines the RD-WR command spacing, in terms of common clocks based on the following formula: CL + 0.5xBL + TA (RD-WR) – DQSS DQSS: is time from Write command to data and is always 1 CK BL: is Burst Length which is set to 4 TA (RD-WR): is required DQ turn-around, can be set to 1, 2 or 3 CK CL: is CAS latency, can be set to 2 or 2.5 **Examples of usage**: For BL=4, with single DQ turn-around and CL=2, this field must be set to 4 CK (2+2+1-1) **Encoding CK between RD and WR commands** 00: 7 01: 6 10: 5 11: 4 **NOTE:** Since reads in DDR SDRAM cannot be terminated by Writes, the Space between commands is not a function of Cycle Length but of Burst Length.
25	**Back To Back Read-Read commands spacing (DDR, different Rows):** This field determines the RD-RD Command Spacing, in terms of common clocks based on the following formula: 0.5xBL + TA(RD-RD) BL: is Burst Length and can be set to 4. TA (RD-RD): is required DQ turn-around, can be set to 1 or 2 CK **Examples of usage**: For BL=4, with single DQ turn-around, this field must be set to 3 CK (2+1) **Encoding CK between RD and RD commands** 0: 4 1: 3 **NOTE:** Since a Read to a different row does not terminate a Read, the Space between commands is not a function of Cycle Length but of Burst Length.
24:15	**Reserved**
14:12	**Refresh Cycle Time (tRFC)**: Refresh Cycle Time is measured for a given row from REF command (to perform a refresh) until following ACT to same row (to perform a Read or Write). It is tracked separately from tRC for DDR SDRAM. Current DDR SDRAM spec requires tRFC of 75 ns (DDR266) and 80 ns (DDR200). Therefore, this field will be set to 8 clocks for DDR200, 10 clocks for DDR266. **Encoding tRFC** 000: 14 clocks 001: 13 clocks 010: 12 clocks 011: 11 clocks 100: 10 clocks 101: 9 clocks 110: 8 clocks 111: 7 clocks

11	**Activate to Precharge delay (tRAS), MAX**: This bit controls the maximum number of clocks that a DDR SDRAM bank can remain open. After this time period, the system memory Controller will guarantee to pre-charge the bank. Note that this time period may or may not be set to overlap with time period that requires a refresh to happen. The DDR SDRAM Controller includes a separate tRAS-MAX counter for every supported bank. With a maximum of four rows and four banks per row, there are 16 counters. 0: 120 micro-seconds 1: Reserved.
10:9	**Activate to Precharge delay (tRAS), MIN**: This bit controls the number of DDR SDRAM clocks for tRAS MIN 00: 8 Clocks 01: 7 Clocks 10: 6 Clocks 11: 5 Clocks
8:7	**Reserved**
6:5	**CAS# Latency (tCL)**: Encoding DDR SDRAM CL 00: 2.5 01: 2 10: Reserved 11: Reserved
4	**Reserved**
3:2	**DDR SDRAM RAS# to CAS# Delay (tRCD):** This bit controls the number of clocks inserted between a Row Activate command and a Read or Write command to that row. Encoding tRCD 00: 4 DDR SDRAM Clocks (DDR 333 SDRAM) 01: 3 DDR SDRAM Clocks 10: 2 DDR SDRAM Clocks 11: Reserved
1:0	**DDR SDRAM RAS# Precharge (tRP):** This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same row. Encoding tRP 00: 4 DDR SDRAM Clocks (DDR 333 SDRAM) 01: 3 DDR SDRAM Clocks 10: 2 DDR SDRAM Clocks 11: Reserved

4.9.15 PWRMG – DRAM Controller Power Management Control Register (Device #0)

Address Offset:	68-6Bh
Default Value:	00000000h
Access:	Read/Write
Size:	32 bits

Bit	Description
31:24	**Reserved**
23:20	**Row State Control:** This field determines the number of clocks the System Memory Controller will remain in the idle state before it begins pre-charging all pages or powering down rows. **- PDEn: Power Down Enable** **- PCEn: Page Close Enable** **- TC: Timer Control** **PDEn(23):** / PCEn(22): / TC(21:20) / Function 0 / 0 / XX / All Disabled 0 / 1 / XX / Reserved 1 / 0 / XX / Reserved 1 / 1 / 00 / Immediate Precharge and Powerdown 1 / 1 / 01 / Reserved 1 / 1 / 10 / Precharge and Power Down after 16 DDR SDRAM Clocks 1 / 1 / 11 / Precharge and Power Down after 64 DDR SDRAM Clocks
19:16	**Reserved**
15	**Self Refresh GMCH Memory Interface Data Bus Power Management Optimization Enable**: 0 = Enable 1 = Disable
14	**CS# Signal Drive Control**: 0 = Enable CS# Drive Control, based on rules described in DRC bit 12. 1 = Disable CS# Drive Control, based on rules described in DRC bit 12.
13	**Self Refresh GMCH Memory Interface Data Bus Power Management**: 0 = In Self Refresh Mode GMCH Power Management is Enabled. 1 = In Self Refresh Mode the GMCH Power Management is Disabled.
12	**Dynamic Memory Interface Power Management**: 0 = Dynamic Memory Interface Power Management Enabled. 1 = Dynamic Memory Interface Power Management Disabled.
11	**Rcven DLL shutdown disable**: 0 = Normal operation. RCVEN DLL is turned off when the corresponding SO-DIMM is unpopulated. 1 = RCVEN DLL is turned on irrespective of SO-DIMM population.

10	**Reserved**.
9:1	**Reserved**
0	**Power State S1/S3 Refresh Control**: 0 = Normal Operation, Pending refreshes are not completed before entering Self Refresh for S1/S3. 1 = All Pending Refreshes plus one extra is performed before entering Self Refresh for S1/S3.

4.9.16 DRC – DRAM Controller Mode Register (Device #0)

Address Offset: 70-73h
Default Value: 00000081h
Access: RO, Read/Write
Size: 32 bits

Bit	Description
31:30	**Revision Number (REV):** Reflects the revision number of the format used for DDR SDRAM register definition (Read Only).
29	**Initialization Complete (IC):** This bit is used for communication of software state between the Memory Controller and the BIOS. BIOS sets this bit to 1 after initialization of the DDR SDRAM Memory Array is complete. Setting this bit to a 1 enables DDR SDRAM Refreshes. On power up and S3 exit, the BIOS initializes the DDR SDRAM array and sets this bit to a 1. This bit works in combination with the RMS bits in controlling Refresh state: IC Refresh State 0 OFF 1 ON
28:24	**Reserved**
23:22	**Number of Channels (CHAN):** Reflects that GMCH supports only one system memory channel. 00: One channel is populated appropriately Others: Reserved
21:20	**DDIM DDR SDRAM Data Integrity Mode**: 00: ECC is not supported on this system. Thus, no read-merge-write on partial writes. ECC data sense-amps are disabled and the data output is tristate (Default). XX: Reserved
19:16	**Reserved**
15	**RAS Lock-Out Enable:** Set to a 1 if all populated rows support RAS Lock-Out. Defaults to 0. If this bit is set to a 1 the DDR SDRAM Controller assumes that the DDR SDRAM guarantees tRAS min before an auto precharge (AP) completes (Note: An AP is sent with a Read or a Write command). Also, the DDR SDRAM Controller does not issue an activate command to the auto pre-charged bank for tRP. If this bit is set to a 0 the DDR SDRAM Controller does not schedule an AP if tRAS min is not met.
14:13	**Reserved**
12	**Address Tri-state enable (ADRTRIEN):** When set to a 1, the SDRAM Controller will tri-state the MA, CMD, and CS# (only when all CKEs are deasserted). Note that when CKE to a row is deasserted, fast chip select assertion is not permitted by the hardware. CKEs deassert based on Idle Timer and/or max row count control. 0: Address Tri-state Disabled 1: Address Tri-state Enabled
11:10	**Reserved**

9:7	**Refresh Mode Select (RMS)**: This field determines whether Refresh is enabled and, if so, at what rate Refreshes will be executed. **000:** Refresh disabled **001:** Refresh enabled. Refresh interval 15.6 µsec **010:** Refresh enabled. Refresh interval 7.8 µsec **011:** Reserved. **111:** Refresh enabled. Refresh interval 64 clocks (fast refresh mode) **Other:** Reserved Any change in the programming of this field Resets the Refresh counter to zero. This function is for testing purposes, it allows test program to align refresh events with the test and thus improve failure repeatability.

6:4	**Mode Select (SMS).** These bits select the special operational mode of the DDR SDRAM Interface. The special modes are intended for initialization at power up. **000:** Post Reset State – When the GMCH exits Reset (power-up or otherwise), the mode select field is cleared to 000. Software is not expected to Write this value, however if this value is Written, there are no side effects (no Self Refresh or any other special DDR SDRAM cycle). During any Reset sequence, while power is applied and Reset is active, the GMCH deasserts all CKE signals. After internal Reset is deasserted, CKE signals remain deasserted until this field is written to a value different than 000. On this event, all CKE signals are asserted. During Suspend (S3, S4), GMCH internal signal triggers DDR SDRAM Controller to flush pending commands and enter all rows into Self-Refresh mode. As part of Resume sequence, GMCH will be Reset , which will clear this bit field to 000 and maintain CKE signals deasserted. After internal Reset is deasserted, CKE signals remain deasserted until this field is Written to a value different than 000. On this event, all CKE signals are asserted. During Entry to other low power states (C3, S1-M), GMCH internal signal triggers DDR SDRAM Controller to flush pending commands and enter all rows in S1 and relevant rows in C3 (Based on RPDNC3) into Self-Refresh mode. During exit to Normal mode, the GMCH signal triggers DDR SDRAM Controller to Exit Self-Refresh and Resume Normal operation without S/W involvement. **001:** NOP Command Enable – All CPU cycles to DDR SDRAM result in a NOP command on the DDR SDRAM interface. **010:** All Banks Pre-charge Enable – All CPU cycles to DDR SDRAM result in an All Banks Precharge command on the DDR SDRAM interface. **011:** Mode Register Set Enable – All CPU cycles to DDR SDRAM result in a Mode Register set command on the DDR SDRAM Interface. Host address lines are mapped to DDR SDRAM address lines in order to specify the command sent. Host address HA[13:3] are mapped to Memory address SMA[11,9:0]. SMA3 must be driven to 1 for interleave wrap type. **For Double Data Rate** MA[6:4] needs to be driven based on the value programmed in the CAS# Latency field. CAS Latency MA[6:4] 1.5 Clocks 001 2.0 Clocks 010 2.5 Clocks 110 SMA[7] should always be driven to a 0. SMA[8] Should be driven to a 1 for DLL Reset and 1 for Normal Operation. SMA[12:9] must be driven to 00000. BIOS must calculate and drive the correct host address for each row of Memory such that the correct command is driven on the SMA[12:0] lines. Note that SMAB[5,4,2,1]# are inverted from SMA[5,4,2,1]; BIOS must account for this. **100:** Extended Mode Register Set Enable – All CPU cycles to DDR SDRAM result in an "Extended Mode register set" command on the DDR SDRAM Interface. Host address lines are mapped to DDR SDRAM address lines in order to specify the command sent. Host address lines are mapped to DDR SDRAM address lines in order to specify the command sent. Host address HA[13:3] are mapped to Memory address SMA[11,9:0]. SMA[0] = 0 for DLL enable and 1 for DLL disable. All the other SMA lines are driven to 0's. Note that SMAB[5,4,2,1]# are inverted from SMA[5,4,2,1]; BIOS must account for this. **101**: Reserved **110:** CBR Refresh Enable – In this mode all CPU cycles to DDR SDRAM result in a CBR cycle on the DDR SDRAM interface **111:** Normal operation
3:0	**Reserved**

4.9.17 DTC – DRAM Throttling Control Register (Device #0)

Address Offset:	A0-A3h
Default Value:	00000000h
Access:	Read/Write/Lock
Size:	32 bits

Throttling is independent for system memory banks, GMCH Writes, and Thermal Sensor Trips. Read and Write Bandwidth is measured independently for each bank. If the number of Octal - Words (16 bytes) Read/Written during the window defined below (Global DDR SDRAM Sampling Window: GDSW) exceeds the DDR SDRAM Bandwidth Threshold, then the DDR SDRAM Throttling mechanism will be invoked to limit DDR SDRAM Reads/Writes to a lower bandwidth checked over smaller time windows. The throttling will be active for the remainder of the current GDSW and for the next GDSW after which it will return to Non-Throttling mode. The throttling mechanism accounts for the actual bandwidth consumed during the sampling window, by reducing the allowed bandwidth within the smaller throttling window based on the bandwidth consumed during the sampling period. Although bandwidth from/to independent rows and GMCH Write bandwidth is measured independently, once Tripped all transactions except high priority graphics Reads are subject to throttling.

Bit	Description
31:28	**DDR SDRAM Throttle Mode (TMODE)**: Four bits control which mechanisms for Throttling are enabled in an “OR” fashion. Counter-based Throttling is lower priority than Thermal Trips Throttling when both are enabled and Tripped. Counter-based trips point Throttling values and Thermal-based Trip Point Throttling values are specified in this register. If the counter and thermal mechanisms for either Rank or GMCH are both enabled, Throttle settings for the one that Trips first is used until the end of the second gdsw. [Rank Counter, GMCH Write Counter, Rank Thermal Sensor, GMCH Thermal Sensor] 0000 = Throttling turned off. This is the default setting. All Counters are off. 0001 = Only GMCH Thermal Sensor based Throttling is enabled. If GMCH Thermal Sensor is Tripped, Write Throttling begins based on the setting in WTTC. 0010 = Only Rank Thermal Sensor based Throttling is enabled. When the external SO-DIMM Thermal sensor is Tripped, DDR SDRAM Throttling begins based on the setting in RTTC. 0011 = Both Rank and GMCH Thermal Sensor based throttling is enabled. When the external SO-DIMM Thermal Sensor is Tripped DDR SDRAM Throttling begins based on the setting in RTTC. If the GMCH Thermal Sensor is Tripped, Write Throttling begins based on the setting in WTTC. 0100 = Only the GMCH Write Counter mechanism is enabled. When the length of write transfers programmed (GDSW * WCTC) is reached, DRAM throttling begins based on the setting in WCTC.. 0101 = GMCH Thermal Sensor and GMCH Write DDR SDRAM Counter mechanisms are both enabled. If the GMCH Write DDR SDRAM Counter mechanism threshold is reached, DDR SDRAM Throttling begins based on the setting in WCTC. If the GMCH Thermal Sensor is tripped, DDR SDRAM Throttling begins based on the setting in WTTC. If both threshold mechanisms are tripped, the DDR SDRAM Throttling begins based on the settings in WTTC. 0110 = Rank Thermal Sensor and GMCH Write DDR SDRAM Counter mechanisms are both enabled. If the GMCH Write DDR SDRAM Counter mechanism threshold is reached, DDR SDRAM Throttling begins based on setting in WCTC. If the external SO-DIMM Thermal Sensor is tripped, Rank DDR SDRAM throttling begins based on the setting in RTTC. 0111 = Similar to 0101 for Writes and when the Rank Thermal Sensor is tripped, DDR SDRAM Throttling begins based on the setting in RTTC. 1000 = Only Rank Counter mechanism is enabled. When the length of read transfers programmed (GDSW * RCTC) is reached, DRAM throttling begins based on the setting in RCTC 1001 = Rank Counter mechanism is enabled and GMCH Thermal Sensor based throttling are both enabled. If GMCH thermal sensor is tripped, write throttling begins based on the setting in WTTC. If the rank counter mechanism is tripped, DRAM throttling begins based on the setting in RCTC. 1010 = Rank Thermal Sensor and Rank DDR SDRAM Counter mechanisms are both enabled. If the rank DDR SDRAM Counter mechanism threshold is reached, DDR SDRAM Throttling begins based on the setting in RCTC. If the external SO-DIMM Thermal Sensor is tripped, DRAM Throttling begins based on the setting in RTTC. 1011 = Similar to 1010 and if the GMCH Thermal Sensor is tripped, Write Throttling begins based on the setting in WTTC. 1111 = Rank and GMCH Thermal Sensor based Throttling and Rank and GMCH Write Counter based Throttling are enabled. If both the Write Counter and GMCH Thermal Sensor based mechanisms are tripped, DDR SDRAM Throttling begins based on the setting allowed in WTTC. If both the Rank Counter and Rank Thermal Sensor based mechanisms are tripped, DDR SDRAM Throttling begins based on the setting allowed in RTTC.

27:24	**Read Counter Based Power Throttle Control (RCTC):** These bits select the Counter based Power Throttle Bandwidth Limits for Read operations to system memory. R/W, RO if Throttle Lock. 0h = 85% 1h = 70% 2h = 65% 3h = 60% 4h = 55% 5h = 50% 6h = 45% 7h = 40% 8h = 35% 9h = 30% Ah = 20% B-Fh = Reserved
23:20	**Write Counter Based Power Throttle Control (WCTC):** These bits select the counter based Power Throttle Bandwidth Limits for Write operations to system memory. R/W, RO if Throttle Lock 0h = 85% 1h = 70% 2h = 65% 3h = 60% 4h = 55% 5h = 50% 6h = 45% 7h = 40% 8h = 35% 9h = 30% Ah = 20% B-Fh = Reserved
19:16	**Read Thermal Based Power Throttle Control (RTTC):** These bits select the Thermal Sensor based Power Throttle Bandwidth Limits for Read operations to system memory. R/W, RO if Throttle Lock. 0h = 85% 1h = 70% 2h = 65% 3h = 60% 4h = 55% 5h = 50% 6h = 45% 7h = 40% 8h = 35% 9h = 30% Ah = 20% B-Fh = Reserved

15:12	**Write Thermal Based Power Throttle Control (WTTC):** These bits select the Thermal based Power Throttle Bandwidth Limits for Write operations to system memory. R/W, RO if Throttle Lock 0h = 85% 1h = 70% 2h = 65% 3h = 60% 4h = 55% 5h = 50% 6h = 45% 7h = 40% 8h = 35% 9h = 30% Ah = 20% B-Fh = Reserved
11	**Counter Based Throttle Lock (CTLOCK):** This bit secures RCTC and WCTC. This bit defaults to 0. Once a 1 is written to this bit, RCTC and WCTC (including CTLOCK) become Read-Only.
10	**Thermal Throttle Lock (TTLOCK):** This bit secures the DDR SDRAM Throttling Control register. This bit defaults to 0. Once a 1 is written to this bit, all of the configuration register bits in DTC (including TTLOCK) except CTLOCK, RCTC and WCTC become Read-Only.
9	**Thermal Power Throttle Control fields Enable**: 0 = RTTC and WTTC are not used. RCTC and WTCT are used for both Counter and Thermal based Throttling. 1 = RTTC and WTTC are used for Thermal based Throttling.
8	**High Priority Stream Throttling Enable**: Normally High Priority Streams are not Throttled when either the counter based mechanism or Thermal Sensor mechanism demands Throttling. 0 = Normal operation. 1 = Block High priority streams during Throttling.
7:0	**Global DDR SDRAM Sampling Window (GDSW):** This 8-bit value is multiplied by 4 to define the length of time in milliseconds (0–1020) over which the number of Octal Words (16 bytes) Read/Written is counted and Throttling is imposed. Note that programming this field to 00h disables system memory throttling. Recommended values are between 0.25 and 0.75 seconds.

4.10 Intel 854 GMCH Configuration Process Registers (Device #0, Function #3)

See "Nomenclature for Access Attributes" on page 42 for access nomenclature. Table 23 summarizes all Device#0, Function #3 registers.

Table 23. Configuration Process Configuration Space (Device#0, Function #3)

Register Name	Register Symbol	Register Start	Register End	Default Value	Access
Vendor Identification	VID	00	01	8086h	RO
Device Identification	DID	02	03	358Ch	RO
PCI Command	PCICMD	04	05	0006h	RO,R/W
PCI Status	PCISTS	06	07	0080h	RO,R/WC
Revision Identification	RID	08	08	02h	RO
Sub-Class Code	SUBC	0A	0A	80h	RO
Base Class Code	BCC	0B	0B	08h	RO
Header Type	HDR	0E	0E	80h	RO
Subsystem Vendor Identification	SVID	2C	2D	0000h	R/WO
Subsystem Identification	SID	2E	2F	0000h	R/WO
Capabilities Pointer	CAPPTR	34	34	00h	RO
HPLL Clock Control	HPLLCC	C0	C1	00h	RO

4.10.1 VID – Vendor Identification Register

Address Offset: 00-01h
Default Value: 8086h
Access: Read Only
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Descriptions
15:0	**Vendor Identification (VID):** This register field contains the PCI standard identification for 8086h.

4.10.2 DID – Device Identification Register

Address Offset:	02-03h
Default Value:	358Ch
Access:	Read Only
Size:	16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Descriptions
15:0	**Device Identification Number (DID):** This is a 16-bit value assigned to the Intel 854 GMCH Host-HI Bridge Function #3 (358Ch).

4.10.3 PCICMD – PCI Command Register

Address Offset:	04-05h
Default Value:	0006h
Access:	Read Only, Read/Write
Size:	16 bits

Since the Intel® 82854 GMCH Device #0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Descriptions
15:10	**Reserved**
9	**Fast Back-to-Back Enable (FB2B):** This bit controls whether or not the master can do fast back-to-back Write. Since Device #0 is strictly a target, this bit is not implemented and is hardwired to 0. Writes to this bit position have no effect.
8	**SERR Enable (SERRE):** SERR# is not implemented by Function #1 of Device #0 of the GMCH and this bit is hardwired to 0. Writes to this bit position have no effect.
7	**Address/Data Stepping Enable (ADSTEP):** Address/data stepping is not implemented in the GMCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	**Parity Error Enable (PERRE):** PERR# is not implemented by GMCH and this bit is hardwired to 0. Writes to this bit position have no effect.
5	**VGA Palette Snoop Enable (VGASNOOP):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	**Memory Write and Invalidate Enable (MWIE):** The GMCH will never issue Memory Write and Invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3	**Special Cycle Enable (SCE):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	**Bus Master Enable (BME):** The GMCH is always enabled as a master on HI. This bit is hardwired to a 1. Writes to this bit position have no effect.
1	**Memory Access Enable (MAE):** The GMCH always allows access to Main Memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	**I/O Access Enable (IOAE):** This bit is not implemented in the GMCH and is hardwired to a 0. Writes to this bit position have no effect.

4.10.4 PCISTS – PCI Status Register

Address Offset:	06-07h
Default Value:	0080h
Access:	Read Only, Read/Write Clear
Size:	16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device #0's PCI Interface. Bit 14 is Read/Write clear. All other bits are Read Only. Since GMCH Device #0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Descriptions
15	**Detected Parity Error (DPE):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
14	**Signaled System Error (SSE):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
13	**Received Master Abort Status (RMAS):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
12	**Received Target Abort Status (RTAS):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
11	**Signaled Target Abort Status (STAS):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
10:9	**DEVSEL Timing (DEVT):** These bits are hardwired to "00". Writes to these bit positions have no affect. Device #0 does not physically connect to PCI_A. These bits are set to "00" (fast decode) so that the GMCH does not limit optimum DEVSEL timing for PCI_A.
8	**Master Data Parity Error Detected (DPD):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
7	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1. Writes to these bit positions have no effect. Device #0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the GMCH does not limit the optimum setting for PCI_A.
6:5	**Reserved**
4	**Capability List (CLIST):** This bit is hardwired to 0 to indicate to the configuration software that this device/function does not implement new capabilities.
3:0	**Reserved**

4.10.5 RID – Revision Identification Register

Address Offset:	08h
Default Value:	02h
Access:	Read Only
Size:	8 bits

This register contains the revision number of the Intel® 82854 GMCH. These bits are Read Only and Writes to this register have no effect.

Bit	Descriptions
7:0	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the GMCH.

4.10.6 SUBC – Sub-Class Code Register

Address Offset:	0Ah
Default Value:	80h
Access:	Read Only
Size:	8 bits

This register contains the Sub-Class Code for the Intel® 82854 GMCH Device #0. This code is 80h indicating a peripheral device.

Bit	Descriptions
7:0	**Sub-Class Code (SUBC)**: This is an 8-bit value that indicates the category of Bridge into which GMCH falls. The code is 80h indicating other peripheral device.

4.10.7 BCC – Base Class Code Register

Address Offset:	0Bh
Default Value:	08h
Access:	Read Only
Size:	8 bits

This register contains the Base Class Code of the Intel® 82854 GMCH Device #0 Function #3. This code is 08h indicating a peripheral device.

Bit	Descriptions
7:0	**Base Class Code (BASEC)**: This is an 8-bit value that indicates the Base Class code for the GMCH. This code has the value 08h, indicating other peripheral device.

4.10.8 HDR – Header Type Register

Address Offset:	0Eh
Default Value:	80h
Access:	Read Only
Size:	8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	**PCI Header (HDR)**: This field always returns 80 to indicate that Device #0 is a multifunction device. If Functions other than #0 are disabled this field returns a 00 to indicate that the GMCH is a single function device with standard header layout. The default is 80 Reads and Writes to this location have no effect.

4.10.9 SVID – Subsystem Vendor Identification Register

Address Offset:	2C-2Dh
Default Value:	0000h
Access:	Read/Write Once
Size:	16 bits

This value is used to identify the vendor of the subsystem.

Bit	Descriptions
15:0	**Subsystem Vendor ID (SUBVID)**: This field should be programmed during boot-up to indicate the vendor of the system board. After it has been Written once, it becomes Read Only.

4.10.10 ID – Subsystem Identification Register

Address Offset:	2E-2Fh
Default Value:	0000h
Access:	Read/Write Once
Size:	16 bits

This value is used to identify a particular subsystem.

Bit	Descriptions
7:0	**Subsystem ID (SUBID)**: This field should be programmed during BIOS initialization. After it has been Written once, it becomes Read Only.

4.10.11 CAPPTR – Capabilities Pointer Register

Address Offset:	34h
Default Value:	00h
Access:	Read Only
Size:	8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Descriptions
7:0	**Pointer to the offset of the first capability ID register block:** In this case there are no capabilities therefore these bits are hardwired to 00h to indicate the end of the capability-linked list.

4.10.12 HPLLCC – HPLL Clock Control Register (Device #0)

Address Offset:	C0-C1h
Default Value:	00h
Access:	Read Only
Size:	16 bits

Bit	Descriptions
15:11	Reserved
10	**HPLL VCO Change Sequence Initiate Bit**: Software must Write a 0 to clear this bit and then Write a 1 to initiate sequence again.
9	Hphase Reset Bit: 1 = Assert 0 = Deassert (default)
8	Reserved
7:2	Reserved
1:0	HPLL Clock Control: Software is allowed to update this register. See Table 24.

Table 24. Intel® 82854 GMCH Configurations and Some Resolution Examples: Native Graphics Mode

Straps Read Through HPLLCC[2:0]: D0:F3:Register Offset C0-C1h, bits[2:0]	FSB Rate	System Memory Frequency	GFX Core Clock(Low) GFX Core Clock (High)	DVO Port	CRT Port
000	400 MHz	266 MHz	200 MHz	1600x1200@85 Hz DCLK = 229- MHz	1600x1200@85-Hz DCLK = 229 -MHz
				2048x1536@72 Hz DCLK = 324 MHz	2048x1536@75 Hz DCLK = 340 MHz
111	400 MHz	333 MHz	250 MHz	1600x1200@85 Hz DCLK = 229 MHz	1600x1200@85 Hz DCLK = 229 MHz
				2048x1536@72 Hz DCLK = 324 MHz	2048x1536@75 Hz DCLK = 340 MHz

4.11 Intel® 82854 GMCH Integrated Graphics Device Registers (Device #2, Function #0)

This section contains the PCI configuration registers listed in order of ascending offset address. Device #2 incorporates Function #0. See "Nomenclature for Access Attributes" on page 42 for access nomenclature.

Note: C0F0 = Copy of Function #0 and U1F1 = Unique in Function #1.

Table 25. Integrated Graphics Device Configuration Space (Device #2, Function#0)

Register Name	Register Symbol	Address Offset	Register End	Default Value	Access	Regs in Function#1
Vendor Identification	VID	00h	01h	8086h	RO	C0F0
Device Identification	DID	02h	03h	358Eh	RO	C0F0
PCI Command	PCICMD	04h	05h	0000h	RO,R/W	U1F1
PCI Status	PCISTS	06h	07h	0090h	RO	U1F1
Revision Identification	RID	08h	08h	02h	RO	C0F0
Class Code	CC	09h	0Bh	030000h	RO	U1F1
Cache Line Size	CLS	0Ch	0Ch	00h	RO	C0F0
Master Latency Timer	MLT	0Dh	0Dh	00h	RO	C0F0
Header Type	HDR	0Eh	0Eh	00h	RO	C0F0
Graphics Memory Range Address	GMADR	10h	13h	00000008h	RO,R/W	U1F1
Memory Mapped Range Address	MMADR	14h	17h	00000000h	RO,R/W	U1F1
IO Range	IOBAR	18h	1Bh	00000001h	RO,R/W	–
Subsystem Vendor ID	SVID	2Ch	2Dh	0000h	R/WO	C0F0
Subsystem ID	SID	2Eh	2Fh	0000h	R/ WO	C0F0
Video Bios ROM Base Address	ROMADR	30h	33h	00000000h	RO	C0F0
Interrupt Line	INTRLINE	3Ch	3Ch	00h	RO in F#1, R/W	–
Interrupt Pin	INTRPIN	3Dh	3Dh	01h	RO, Reserved In F#1	–
Minimum Grant	MINGNT	3Eh	3Eh	00h	RO	C0F0
Maximum Latency	MAXLAT	3Fh	3Fh	00h	RO	C0F0
Power Management Capabilities	PMCAP	D2h	D3h	0221h	RO	C0F0
Power Management Control	PMCS	D4h	D5h	0000h	RO,R/W	U1F1

4.11.1 VID – Vendor Identification Register (Device #2)

Address Offset:	00-01h
Default Value:	8086h
Access:	Read Only
Size:	16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number:** This is a 16-bit value assigned to Intel.

4.11.2 DID – Device Identification Register (Device #2)

Address Offset:	02-03h
Default Value:	358Eh
Access:	Read Only
Size:	16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number:** This is a 16-bit value assigned to the GMCH IGD (358Eh).

4.11.3 PCICMD – PCI Command Register (Device #2)

Address Offset:	04-05h
Default Value:	0000h
Access:	Read Only, Read/Write
Size:	16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD register in the IGD disables the IGD PCI compliant master accesses to main system memory.

Bit	Description
15:10	**Reserved**
9	**Fast Back-to-Back (FB2B)–RO**
8	**SERR# Enable (SERRE) –RO**
7	**Address/Data Stepping–RO**
6	**Parity Error Enable (PERRE) –RO**
5	**Video Palette Snooping (VPS) –RO**
4	**Memory Write and Invalidate Enable (MWIE) –RO**
3	**Special Cycle Enable (SCE) –RO**
2	**Bus Master Enable (BME) –R/W:** This bit determines if the IGD is to function as a PCI compliant master. 0= Disable IGD bus mastering (default). 1 = Enable IGD bus mastering.
1	**Memory Access Enable (MAE) –R/W:** This bit controls the IGD's response to System Memory Space accesses. 0= Disable (default). 1 = Enable.
0	**I/O Access Enable (IOAE) –R/W:** This bit controls the IGD's response to I/O Space accesses. 0 = Disable (default). 1 = Enable.

4.11.4 PCISTS – PCI Status Register (Device #2)

Address Offset:	06-07h
Default Value:	0090h
Access:	Read Only
Size:	16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Description
15	**Detected Parity Error (DPE):** Since the IGD does not detect parity, this bit is always set to 0.
14	**Signaled System Error (SSE) – RO**
13	**Received Master Abort Status (RMAS) – RO**
12	**Received Target Abort Status (RTAS) – RO**
11	**Signaled Target Abort Status (STAS) – RO**
10:9	**DEVSEL# Timing (DEVT) – RO**
8	**Data Parity Detected (DPD) – RO**
7	**Fast Back-to-Back (FB2B) – RO**
6	**User Defined Format (UDF) – RO**
5	**66-MHz PCI Capable (66C) – RO**
4	**CAP LIST:** This bit is set to 1 to indicate that the register at 34h provides an offset into the Function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3:0	**Reserved**

4.11.5 RID – Revision Identification Register (Device #2)

Address Offset:	08h
Default Value:	02h
Access:	Read Only
Size:	8 bits

This register contains the revision number of the IGD. These bits are Read Only and Writes to this register have no effect.

Bit	Description
7:0	**Revision Identification Number:** This is an 8-bit value that indicates the revision identification number for the GMCH.

4.11.6 CC – Class Code Register (Device #2)

Address Offset:	09-0Bh
Default Value:	030000h
Access:	Read Only
Size:	24 bits

This register contains the device programming interface information related to the Sub-Class code and Base Class code definition for the IGD. This register also contains the Base Class code and the function sub-class in relation to the Base Class code.

Bit	Description
23:16	**Base Class Code (BASEC):** 03=Display controller
15:8	Sub-Class Code (SCC): Function 0: 00h=VGA compatible or 80h=Non VGA Function 1: 80h=Non VGA
7:0	**Programming Interface (PI):** 00h=Hardwired as a Display controller.

4.11.7 CLS – Cache Line Size Register (Device #2)

Address Offset:	0Ch
Default Value:	00h
Access:	Read Only
Size:	8 bits

The IGD does not support this register as a PCI slave.

Bit	Description
7:0	**Cache Line Size (CLS) – RO**

4.11.8 MLT – Master Latency Timer Register (Device #2)

Address Offset:	0Dh
Default Value:	00h
Access:	Read Only
Size:	8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Description
7:0	Master Latency Timer Count Value – RO

4.11.9 HDR – Header Type Register (Device #2)

Address Offset:	0Eh
Default Value:	00h
Access:	Read Only
Size:	8 bits

This register contains the Header Type of the IGD.

Bit	Description
7	**Multi Function Status (MFunc):** Indicates if the device is a multi-function device.
6:0	**Header Code (H):** This is a 7-bit value that indicates the Header code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

4.11.10 GMADR – Graphics Memory Range Address Register (Device #2)

Address Offset:	10-13h
Default Value:	00000008h
Access:	Read/Write, Read Only
Size:	32 bits

IGD graphics system memory base address is specified in this register.

Bit	Description
31:27	**Memory Base Address–R/W:** Set by the OS, these bits correspond to address signals [31:26].
26	**128-MB Address Mask – RO:** 0 indicates 128-MB address
25:4	**Address Mask–RO:** Indicates (at least) a 32-MB address range.
3	**Prefetchable Memory–RO:** Enable prefetching.
2:1	**Memory Type–RO:** Indicates 32-bit address.
0	**Memory/IO Space–RO:** Indicates System Memory Space.

4.11.11 MMADR – Memory Mapped Range Address Register (Device #2)

Address Offset:	14-17h
Default Value:	00000000h
Access:	Read/Write, Read Only
Size:	32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512-kB and the base address is defined by bits [31:19].

Bit	Description
31:19	**Memory Base Address–R/W:** Set by the OS, these bits correspond to address signals [31:19].
18:4	**Address Mask–RO:** Indicate 512-kB address range.
3	**Prefetchable Memory–RO:** Prevents prefetching.
2:1	**Memory Type–RO:** Indicates 32-bit address.
0	**Memory / IO Space–RO:** Indicates System Memory space.

4.11.12 IOBAR – I/O Base Address Register (Device #2)

Address Offset:	18-1Bh
Default Value:	00000001h
Access:	Read/Write
Size:	32 bits

This register provides the Base offset of the I/O registers within Device #2. Bits 15:3 are programmable allowing the I/O Base to be located anywhere in 16-bit I/O Address Space. Bits 2:1 are fixed and return zero, bit 0 is hardwired to a one indicating that 8-bytes of I/O space are decoded.

Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if internal graphics is disabled. Note that access to this IO BAR is independent of VGA functionality within Device #2. Also note that this mechanism is available only through Function #0 of Device#2 and is not duplicated in Function #1.

If accesses to this I/O bar are allowed, then the GMCH claims all 8-bit, 16-bit, or 32-bit I/O cycles from the CPU that falls within the 8B claimed.

Bit	Description
31:16	**Reserved**
15:3	**IO Base Address–R/W:** Set by the OS, these bits correspond to address signals [15:3].
2:1	**Memory Type–RO:** Indicates 32-bit address.
0	**Memory / IO Space–RO**

4.11.13 SVID – Subsystem Vendor Identification Register (Device #2)

Address Offset:	2C-2Dh
Default Value:	0000h
Access:	Read/Write Once
Size:	16 bits

Bit	Description
15:0	**Subsystem Vendor ID:** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a reset.

4.11.14 SID – Subsystem Identification Register (Device #2)

Address Offset:	2E-2Fh
Default Value:	0000h
Access:	Read/Write Once
Size:	16 bits

Bit	Description
15:0	**Subsystem Identification:** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a reset.

4.11.15 ROMADR – Video BIOS ROM Base Address Registers (Device #2)

Address Offset:	30-33h
Default Value:	00000000h
Access:	Read Only
Size:	32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0's.

Bit	Description
31:18	**ROM Base Address–RO**
17:11	**Address Mask–RO:** Indicates 256-kB address range.
10:1	**Reserved**
0	**ROM BIOS Enable–RO:** Indicates ROM not accessible.

4.11.16 INTRLINE – Interrupt Line Register (Device #2)

Address Offset: 3Ch
Default Value: 00h
Access: Read/Write
Size: 8 bits

Bit	Description
7:0	**Interrupt Connection:** Used to communicate interrupt line routing information. POST software Writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the System Interrupt controller that the device's interrupt pin is connected to.

4.11.17 INTRPIN – Interrupt Pin Register (Device #2)

Address Offset: 3Dh
Default Value: 01h
Access: Read Only
Size: 8 bits

Bit	Description
7:0	**Interrupt Pin**: As a single function device, the IGD specifies INTA# as its interrupt pin. 01h=INTA#. For Function #1, this register is set to 00h.

4.11.18 MINGNT – Minimum Grant Register (Device #2)

Address Offset: 3Eh
Default Value: 00h
Access: Read Only
Size: 8 bits

Bit	Description
7:0	**Minimum Grant Value**: The IGD does not burst as a PCI compliant master.

4.11.19 MAXLAT – Maximum Latency Register (Device #2)

Address Offset:	3Fh
Default Value:	00h
Access:	Read Only
Size:	8 bits

Bit	Description
7:0	**Maximum Latency Value**: Bits[7:0]=00h. The IGD has no specific requirements for how often it needs to access the PCI bus.

4.11.20 PMCAP – Power Management Capabilities Register (Device #2)

Address Offset:	D2-D3h
Default Value:	0221h
Access:	Read Only
Size:	16 bits

Bit	Description
15:11	**PME Support:** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10:6	**Reserved**
5	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	**Auxiliary Power Source:** Hardwired to 0.
3	**PME Clock:** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	**Version:** Hardwired to 001b to indicate there are 4 bytes of power management registers implemented.

4.11.21 PMCS – Power Management Control/Status Register (Device #2)

Address Offset:	D4-D5h
Default Value:	0000h
Access:	Read/Write, Read Only
Size:	16 bits

Bit	Description
15	**PME_Status –RO:** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:9	**Reserved**
8	**PME_En–RO:** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	**Reserved**
1:0	**PowerState–R/W:** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to Write an unsupported state to this field, Write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally Reset to initial values. **Bits[1:0] Power State** 00 D0 Default 01 D1 10 D2 Not Supported 11 D3

5.0 Intel® 82854 GMCH System Address Map

A system based on the GMCH supports 4 GB of addressable system memory space and 64 kB+3B of addressable I/O space. The I/O and system memory spaces are divided by system configuration software into regions. The system memory ranges are useful either as system memory or as specialized system memory, while the I/O regions are used solely to control the operation of devices in the system.

When the GMCH receives a Write request whose address targets an invalid space, the data is ignored. For Reads, the GMCH responds by returning all zeros on the requesting interface.

5.1 System Memory Address Ranges

The GMCH provides a maximum system memory of 2 GB. The GMCH does not remap APIC memory space and does not limit DDR SDRAM space in hardware. It is the BIOS or system designer's responsibility to limit system memory population so that adequate PCI High BIOS and APIC memory space can be allocated. Figure 5 and Figure 6 depict the system memory address map in a simplified form and provide details on mapping specific system memory regions as defined and supported by the GMCH.

Figure 5. Simplified View of System Address Map

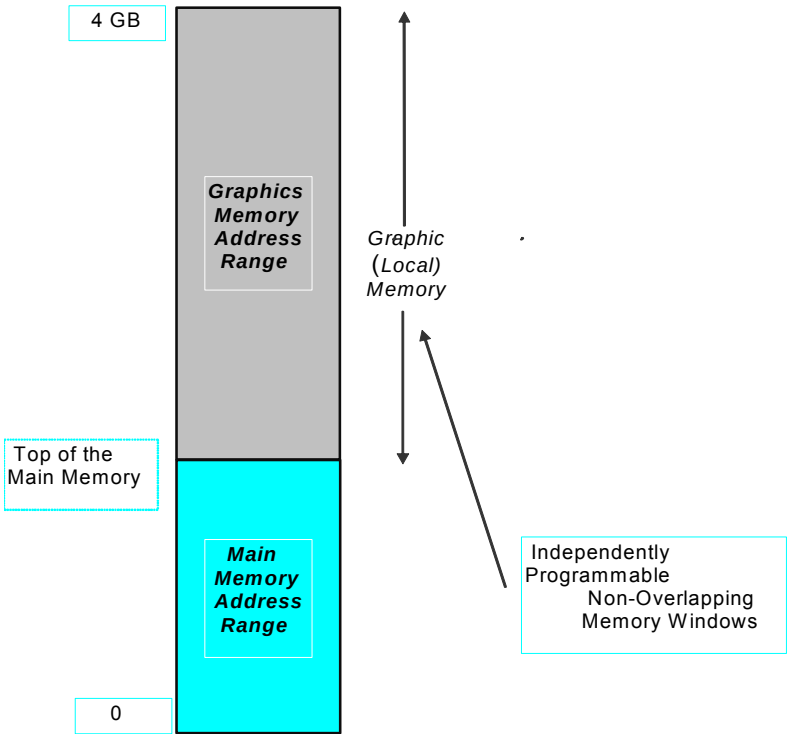
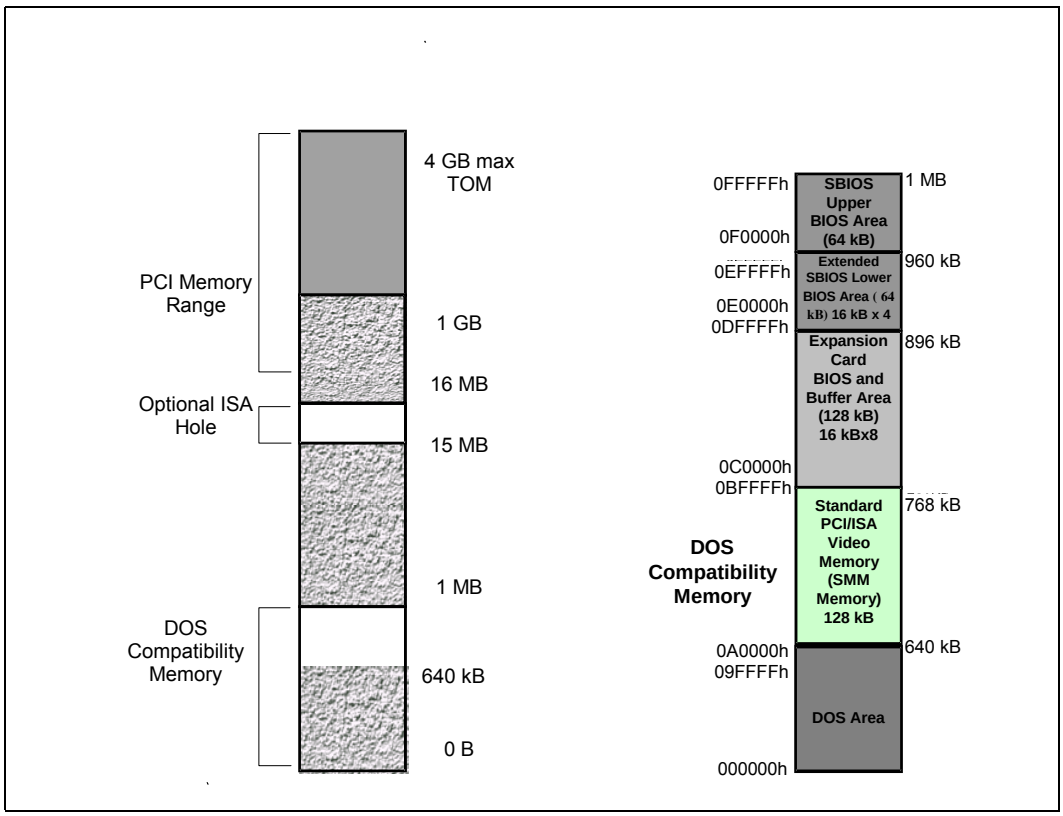


Figure 6. Detailed View of System Address Map



5.2 DOS Compatibility Area

This compatibility region is divided into the following address regions:

- 0 - 640 kB DOS Area
- 640 - 768 kB Video Buffer Area
- 768 - 896 kB in 16-kB sections (total of eight sections) - expansion area
- 896 -960 kB in 16-kB sections (total of four sections) - extended system BIOS area
- 960 kB - 1 MB system BIOS area

There are 16 system memory segments in the compatibility area. Thirteen of the system memory ranges can be enabled or disabled independently for both Read and Write cycles.

Table 26. System Memory Segments and Their Attributes

System Memory Segments	Attributes	Comments
000000H - 09FFFFH	Fixed - always mapped to main DDR SDRAM	0 to 640 kB – DOS Region
0A0000H - 0BFFFFH	Mapped to Hub interface or IGD - configurable as SMM space	Video Buffer (physical DDR SDRAM configurable as SMM space)
0C0000H - 0C3FFFH	WE(Write Enable) RE (Read Enable)	Add-on BIOS
0C4000H - 0C7FFFH	WE RE	Add-on BIOS
0C8000H - 0CBFFFH	WE RE	Add-on BIOS
0CC000H - 0CFFFFH	WE RE	Add-on BIOS
0D0000H - 0D3FFFH	WE RE	Add-on BIOS
0D4000H - 0D7FFFH	WE RE	Add-on BIOS
0D8000H - 0DBFFFH	WE RE	Add-on BIOS
0DC000H - 0DFFFFH	WE RE	Add-on BIOS
0E0000H - 0E3FFFH	WE RE	BIOS Extension
0E4000H - 0E7FFFH	WE RE	BIOS Extension
0E8000H - 0EBFFFH	WE RE	BIOS Extension
0EC000H - 0EFFFFH	WE RE	BIOS Extension
0F0000H - 0FFFFFH	WE RE	BIOS Area

DOS Area (000000h-09FFFFh)

The DOS area is 640 kB in size and is always mapped to the main system memory controlled by the GMCH.

Legacy VGA Ranges (0A0000h-0BFFFFh)

Legacy VGA ranges is accessible when the Intel® 82854 GMCH is strapped into Native Graphics mode. The legacy 128-kB VGA memory range A0000h-BFFFFh (VGA Frame Buffer) can be mapped to IGD (Device #2) and to the Hub interface depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the GMCH always decodes internally mapped devices first. Internal to the GMCH, decode precedence is always given to IGD. The GMCH always positively decodes internally mapped devices, namely the IGD. Subsequent decoding of regions mapped to the Hub interface depends on the Legacy VGA configurations bits (VGA Enable and MDAP). This region is also the default for SMM space.

Compatible SMRAM Address Range (0A0000h-0BFFFFh)

When compatible SMM space is enabled, SMM-mode CPU accesses to this range are routed to physical DDR SDRAM at this address. Non-SMM-mode CPU accesses to this range are considered to be to the video buffer area as described above. Hub interface originated cycles to enabled SMM space are not allowed and are considered to be to the video buffer area.

Monochrome Display Adapter (MDA) Range (0B0000h - 0B7FFFh)

Monochrome Display Adapter ranges is accessible when the Intel® 854 Chipset is strapped into Native Graphics mode. Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD and the Hub interface (depending on configuration bits). Since the monochrome adapter may be mapped to anyone of these devices, the GMCH must decode cycles in the MDA range and forward them either to IGD or to Hub interface. This capability is controlled by a VGA steering bits and the legacy configuration bit (MDAP bit). In addition to the system memory range B0000h to B7FFFh, the GMCH decodes IO cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, and 3BFh and forwards them to either the IGD or the Hub interface.

Expansion Area (0C0000h-0DFFFFh)

This 128-kByte ISA Expansion region is divided into eight, 16-kB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through GMCH and are subtractively decoded to ISA space. System memory that is disabled is not remapped.

Extended System BIOS Area (0E0000h-0EFFFFh)

This 64-kByte area is divided into four, 16-kB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DDR SDRAM or to Hub interface. Typically, this area is used for RAM or ROM. System memory segments that are disabled are not remapped elsewhere.

System BIOS Area (0F0000h-0FFFFFh)

This area is a single 64-kB segment. This segment can be assigned Read and Write attributes. It is by default (after Reset) Read/Write disabled and cycles are forwarded to Hub interface. By manipulating the Read/Write attributes, the GMCH can "shadow" BIOS into the main DDR SDRAM. When disabled, this segment is not remapped.

5.3 Extended System Memory Area

This system memory area covers 100000h (1 MB) to FFFFFFFFh (4 GB-1) address range and it is divided into the following regions:

- Main system memory from 1 MB to the top of system memory.
- PCI Memory space from the top of system memory to 4 GB with two specific ranges.
- APIC Configuration Space from FEC0_0000h (4 GB-20 MB) to FECF_FFFFh (4 GB-19 MB - 1) and FEE0_0000h (4 GB-18 MB) to FEEF_FFFFh (4 GB-17 MB-1).
- High BIOS area from 4 GB to 4 GB - 2 MB

5.4 Main System Memory Address Range (0010_0000h to Top of Main Memory)

The address range from 1 MB to the top of main system memory is mapped to main DDR SDRAM address range controlled by the GMCH. The GMCH will forward all accesses to addresses within this range to the DDR SDRAM unless a hole in this range is created using the fixed hole as controlled by the FDHC register. Accesses within this hole are forwarded to Hub interface.

The GMCH provides a maximum DDR SDRAM address decode space of 4-GB. The GMCH does not remap APIC memory space. The GMCH does not limit DDR SDRAM address space in hardware.

5.4.1 15 MB-16 MB Window

A hole can be created at 15 MB-16 MB as controlled by the fixed hole enable (FDHC register) in Device 0 space. Accesses within this hole are forwarded to the Hub interface. The range of physical DDR SDRAM disabled by opening the hole is not remapped to the top of the memory – that physical DDR SDRAM space is not accessible. This 15 MB-16 MB hole is an optionally enabled ISA hole. Video accelerators originally used this hole. Validation and customer SV teams also use it for some of their test cards. That is why it is being supported. There is no inherent BIOS request for the 15-16 hole.

5.4.2 Pre-allocated System Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOM) are created for SMM-mode and legacy VGA graphics compatibility. It is the responsibility of BIOS to properly initialize these regions. The number of UMA options has been extended. Allocation is at a fixed address in terms of rigid positioning of UMA system memory 'TOM-TSEG-UMA(size), but it is mapped at any available address by a PCI allocation algorithm. GMADR and MMADR are requested through BARs.

The following table details the location and attributes of the regions.

Table 27. Table 33. Pre-allocated System Memory

System Memory Segments	Attributes	Comments
00000000H - 03E7FFFFH	R/W	Available system memory 62.5 -MB
03E80000H - 03F7FFFFH	R/W	Pre-allocated Graphics VGA memory 1-MB (or 4/8/16/32- MB) when IGD is enabled
03F80000H - 03FFFFFFH	SMM Mode Only - CPU Reads	TSEG Address Range
03F80000H - 03FFFFFFH	SMM Mode Only - CPU Reads	TSEG Pre-allocated system memory

5.4.2.1 Extended SMRAM Address Range (HSEG and TSEG)

The HSEG and TSEG SMM transaction address spaces reside in this extended system memory area.

5.4.2.2 HSEG

SMM mode CPU accesses to enabled HSEG are remapped to 000A0000h-000BFFFFh. Non-SMM mode CPU accesses to enabled HSEG are considered invalid are terminated immediately on the FSB. The exceptions to this rule are Non-SMM mode Write Back cycles that are remapped to SMM space to maintain cache coherency. Hub interface originated cycles to enabled SMM space are not allowed. Physical DDR SDRAM behind the HSEG transaction address is not remapped and is not accessible.

5.4.2.3 TSEG

TSEG is 1-MB in size and is at the top of physical system memory. SMM mode CPU accesses to enabled TSEG access the physical DDR SDRAM at the same address. Non-SMM mode CPU accesses to enabled TSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM-mode Write Back cycles that are directed to the physical SMM space to maintain cache coherency. Hub interface originated cycles that enable SMM space are not allowed.

The size of the SMRAM space is determined by the USMM value in the SMRAM register. When the extended SMRAM space is enabled, non-SMM CPU accesses and all other accesses in this range are forwarded to the Hub interface. When SMM is enabled the amount of system memory available to the system is equal to the amount of physical DDR SDRAM minus the value in the TSEG register.

5.4.2.4 Dynamic Video Memory Technology (DVMT)

The IGD supports DVMT in a non-graphics system memory configuration. DVMT is a mechanism that manages system memory and the internal graphics device for optimal graphics performance. DVMT-enabled software drivers, working with the memory arbiter and the operating system, utilize the system memory to support 2D graphics and 3D applications. DVMT dynamically responds to application requirements by allocating the proper amount of display and texturing memory.

5.4.2.5 PCI Memory Address Range (Top of Main System Memory to 4 GB)

The address range from the top of main DDR SDRAM to 4-GB (top of physical system memory space supported by the GMCH) is normally mapped via the Hub interface to PCI.

As an internal graphics configuration, there are two exceptions to this rule.

1. The first exception is addresses decoded to the graphics memory range. One per function in device #2.
2. The second exception is addresses decoded to the system memory mapped range of the Internal Graphics device. One per function in device #2. Both exception cases are forwarded to the Internal Graphics device.

There are two sub-ranges within the PCI Memory address range defined as APIC configuration space and High BIOS Address range. As an Internal Graphics device, the Graphics Memory range and the Memory mapped range of the Internal Graphics device MUST NOT overlap with these two ranges. These ranges are described in detail in the following paragraphs.

5.4.2.6 APIC Configuration Space (FEC0_0000h -FECF_FFFFh, FEE0_0000h- FEEF_FFFFh)

This range is reserved for APIC configuration space that includes the default I/O APIC configuration space. The default Local APIC configuration space is FEE0_0000h to FEEF_0FFFh.

CPU accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the CPU. However, an MTRR must be programmed to make the Local APIC range uncacheable (UC). The Local APIC base address in each CPU should be relocated to the FEC0_0000h (4 GB-20 MB) to FECF_FFFFh range so that one MTRR can be programmed to 64-kB for the Local and I/O APICs. The I/O APIC(s) usually resides in the ICH4-M portion of the chip-set or as a stand-alone component(s).

I/O APIC units will be located beginning at the default address FEC0_0000h. The first I/O APIC will be located at FEC0_0000h. Each I/O APIC unit is located at FEC0_x000h where x is I/O APIC unit number 0 through F(hex). This address range will be normally mapped to Hub interface.

The address range between the APIC configuration space and the High BIOS (FED0_0000h to FFDF_FFFFh) is always mapped to the Hub interface.

5.4.2.7 High BIOS Area (FFE0_0000h -FFFF_FFFFh)

The top 2-MB of the Extended Memory region is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. CPU begins execution from the High BIOS after reset. This region is mapped to Hub interface so that the upper subset of this region aliases to 16 MB to 256-kB range. The actual address space required for the BIOS is less than 2-MB but the minimum CPU MTRR range for this region is 2-MB so that full 2-MB must be considered.

5.4.3 System Management Mode (SMM) Memory Range

The GMCH supports the use of main system memory as System Management RAM (SMM RAM) enabling the use of System Management mode. The GMCH supports three SMM options: Compatible SMRAM (C_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a system memory area that is available for the SMI handler's and code and data storage. This system memory resource is normally hidden from the system OS so that the processor has immediate access to this system memory space upon entry to SMM. The GMCH provides three SMRAM options:

- Below 1-MB option that supports compatible SMI handlers.
- Above 1-MB option that allows new SMI handlers to execute with Write-back cacheable SMRAM.
- Above 1-MByte solutions require changes to compatible SMRAM handlers code to properly execute above 1 MByte.

Note: Hub interface is not allowed to access the SMM space.

5.4.3.1 SMM Space Restrictions

If any of the following conditions are violated the results of SMM accesses are unpredictable and may cause the system to hang:

- The Compatible SMM space must not be set-up as cacheable.
- High or TSEG SMM transaction address space must not overlap address space assigned to DDR SDRAM or to any PCI devices (including Hub interface and graphics devices). This is a BIOS responsibility.
- Both D_OPEN and D_CLOSE must not be set to 1 at the same time.
- When TSEG SMM space is enabled, the TSEG space must not be reported to the OS as available. This is a BIOS responsibility.

5.4.3.2 SMM Space Definition

SMM space is defined by its addressed SMM space and its DDR SDRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the CPU to access SMM space. DDR SDRAM SMM space is defined as the range of physical DDR SDRAM locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High, and TSEG. The Compatible and TSEG SMM space is not remapped and therefore the addressed and DDR SDRAM SMM space is the same address range. Since the High SMM space is remapped the addressed and DDR SDRAM SMM space is a different address range. Note that the High DDR SDRAM space is the same as the Compatible Transaction Address space. Table 28 describes three unique address ranges:

- Compatible Transaction Address (Adr C)
- High Transaction Address (Adr H)
- TSEG Transaction Address (Adr T)

These abbreviations are used later in Table 28.

Table 28. SMM Space Transaction Handling

SMM Space Enabled	Transaction Address Space (Adr)	DRAM Space (DRAM)
Compatible (C)	A0000h to BFFFFh	A0000h to BFFFFh
High (H)	0FEDA0000h to 0FEDBFFFFh	A0000h to BFFFFh
TSEG (T)	(TOM-TSEG_SZ) to TOM	(TOM-TSEG_SZ) to TOM

5.4.4 System Memory Shadowing

Any block of system memory that can be designated as Read-Only or Write-Only can be "shadowed" into GMCH DDR SDRAM. Typically this is done to allow ROM code to execute more rapidly out of main DDR SDRAM. ROM is used as a Read-Only during the copy process while DDR SDRAM at the same time is designated Write-Only. After copying, the DDR SDRAM is designated Read-Only so that ROM is shadowed. CPU bus transactions are routed accordingly.

5.4.5 I/O Address Space

The GMCH does not support the existence of any other I/O devices beside itself on the CPU bus. The GMCH generates Hub interface or PCI bus cycles for all CPU I/O accesses that it does not claim. Within the Host bridge the GMCH contains two internal registers in the CPU I/O space, Configuration Address register (CONFIG_ADDRESS) and the Configuration Data register (CONFIG_DATA). These locations are used to implement Configuration Space Access Mechanism and as described in the Configuration register section.

The CPU allows 64 kB +3 B to be addressed within the I/O space. The GMCH propagates the CPU I/O address without any translation on to the destination bus and therefore provides addressability for 64 k+3 B locations. Note that the upper three locations can be accessed only during I/O address wrap-around when CPU bus A16# address signal is asserted. A16# is asserted on the CPU bus whenever an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. A16# is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

A set of I/O accesses (other than ones used for configuration space access) is consumed by the internal graphics device if it is enabled. The mechanisms for internal graphics IO decode and the associated control is explained later.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the Hub interface. The GMCH will not post I/O Write cycles to IDE.

5.4.5.1 PCI I/O Address Mapping

The GMCH can be programmed to direct non-memory (I/O) accesses to the PCI bus interface when CPU initiated I/O cycle addresses are within the I/O address range. This range is controlled via the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in GMCH Device #1 configuration space.

Address decoding for this range is based on the following concept. The top 4 bits of the respective I/O Base and I/O Limit registers correspond to address bits A[15:12] of an I/O address. For the purpose of address decoding, the GMCH assumes that lower 12 address bits A[11:0] of the I/O base are zero and that address bits A[11:0] of the I/O limit address are FFFh. This forces the I/O address range alignment to 4-kB boundary and produces a size granularity of 4 kB.

The GMCH positively decodes I/O accesses to AGP I/O address space as defined by the following equation:

```
I/O_Base_Address ≤ CPU I/O Cycle Address ≤ I/O_Limit_Address
```

The effective size of the range is programmed by the plug-and-play configuration software and it depends on the size of I/O space claimed by the AGP device.

In Native Graphics mode, the GMCH also forwards accesses to the Legacy VGA I/O ranges according to the settings in the Device #1 configuration registers BCTRL (VGA Enable) and PCICMD1 (IOAE1), unless a second adapter (monochrome) is present on the Hub interface/PCI (or ISA). The presence of a second graphics adapter is determined by the MDAP configuration bit. When MDAP is set, the GMCH will decode legacy monochrome IO ranges and forward them to the Hub interface. The IO ranges decoded for the monochrome adapter are 3B4h, 3B5h, 3B8h, 3B9h, 3Bah and 3BFh.

Note: The GMCH Device #1 I/O address range registers defined above are used for all I/O space allocation for any devices requiring such a window on PCI. These devices would include the AGP device, PCI-66MHz/3.3V agents, and multifunctional AGP devices where one or more functions are implemented as PCI devices.

The PCICMD1 register can disable the routing of I/O cycles to PCI.

5.4.6 GMCH Decode Rules and Cross-Bridge Address Mapping

The address map described above applies globally to accesses arriving on any of the three interfaces (e.g., Host bus, IGD, and Hub interface).

5.4.7 Hub Interface Decode Rules

The GMCH accepts accesses from Hub interface to the following address ranges:

- All Memory Read and Write accesses to Main DDR SDRAM including PAM region (except SMM space)
- Memory writes to VGA range (Native Graphics Mode only)

All Memory Reads from the Hub interface A that are targeted > 4-GB system memory range will be terminated with Master Abort completion, and all Memory Writes (>4-GB) from the Hub interface will be ignored.

Hub interface system memory accesses that fall elsewhere within the system memory range are considered invalid and will be remapped to system memory address 0h, snooped on the Host Bus, and dispatched to DDR SDRAM. Reads will return all 1's with Master Abort completion. Writes will have BE's deasserted and will terminate with Master Abort if completion is required. I/O cycles will not be accepted. They are terminated with Master Abort completion packets.

5.4.7.1 Hub Interface Accesses to GMCH that Cross Device Boundaries

Hub interface accesses are limited to 256 B (Bytes) but have no restrictions on crossing address boundaries. A single Hub interface request may therefore span device boundaries (DDR SDRAM) or cross from valid addresses to invalid addresses (or visa versa). The GMCH does not support transactions that cross device boundaries. For Reads and for Writes requiring completion, the GMCH will provide separate completion status for each naturally aligned 32-B or 64-B block. If the starting address of a transaction hits a valid address, the portion of a request that hits that target device (DDR SDRAM) will complete normally. The remaining portion of the access that crosses a device boundary (targets a different device than that of the starting address) or hits an invalid address will be remapped to system memory address 0h, snooped on the Host Bus, and dispatched to DDR SDRAM. Reads will return all 1's with Master Abort completion. Writes will have BE's (Byte Enable) deasserted and will terminate with Master Abort if completion is required.

If the starting address of a transaction hits an invalid address the entire transaction will be remapped to system memory address 0h, snooped on the Host Bus, and dispatched to DDR SDRAM. Reads will return all 1's with Master Abort completion. Writes will have BE's deasserted and will terminate with Master Abort if completion is required.

5.4.7.2 Interface Decode Rules

Cycles Initiated Using PCI Protocol

The GMCH does not support any PCI access targeting Hub interface. The GMCH will claim PCI initiated memory read and write transactions decoded to the main DDR SDRAM range. All other memory read and write requests will be master-aborted by the PCI initiator as a consequence of GMCH not responding to a transaction.

Under certain conditions, the GMCH restricts access to the DOS Compatibility ranges governed by the PAM registers by distinguishing access type and destination bus. The GMCH accepts PCI write transactions to the compatibility ranges if the PAM designates DDR SDRAM as writeable. If accesses to a range are not write enabled by the PAM, the GMCH does not respond and the cycle will result in a master-abort. The GMCH accepts PCI read transactions to the compatibility ranges if the PAM designates DDR SDRAM as readable. If accesses to a range are not read enabled by the PAM, the GMCH does not respond and the cycle will result in a master-abort.

If agent on PCI issues an I/O or PCI Special Cycle transaction, the GMCH will not respond and cycle will result in a master-abort. The GMCH will accept PCI configuration cycles to the internal GMCH devices as part of the PCI configuration/co-pilot mode mechanism.

Accesses to GMCH that Cross Device Boundaries

For FRAME# accesses, when a PCI master gets disconnected it will resume at the new address which allows the cycle to be routed to or claimed by the new target. Therefore accesses should be disconnected by the target on potential device boundaries. The GMCH will disconnect PCI transactions on 4-kB boundaries.

SBA accesses are limited to 256 bytes and must hit DDR SDRAM. Accesses are dispatched to DDR SDRAM on naturally aligned 32 byte block boundaries. The portion of the request that hits a valid address will complete normally. The portion of a read access that hits an invalid address will be remapped to address 0h, return data from address 0h, and set the IAAF error flag. The portion of a write access that hits an invalid address will be remapped to memory address 0h with BE's deasserted (effectively dropped "on the floor") and set the IAAF error flag.

6.0 Functional Description

6.1 Host Interface Overview

The GMCH front side bus uses source synchronous transfer for the address and data signals. The address signals are double pumped and two addresses can be generated every bus clock. At 100-MHz bus frequency, the two address signals run at 200 MHz for a maximum address queue rate of 50-M addresses/sec. The data is quad pumped and an entire 64-B cache line can be transferred in two bus clocks. At 100-MHz/133MHz bus frequency, the data signals run at 400 MHz for a maximum bandwidth of 3.2/4.3GB/s. The GMCH supports a 8-deep IOQ (In-Order-Queue) using the Intel Celeron M processor, or Genuine Intel® Processor.

6.2 Dynamic Bus Inversion

The GMCH supports dynamic bus inversion (DBI) when driving and receiving data from the Host Bus. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the power consumption of the GMCH. DINV[3:0]# indicates if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

Table 29. Relation of DBI Bits to Data Bits

DINV[3:0]	Data Bits
DINV[0]#	HD[15:0]#
DINV[1]#	HD[31:16]#
DINV[2]#	HD[47:32]#
DINV[3]#	HD[63:48]#

Whenever the CPU or the GMCH drives data, each 16-bit segment is analyzed. If more than eight of the 16 signals would normally be driven low on the bus the corresponding DINV# signal will be asserted and the data will be inverted prior to being driven on the bus. Whenever the CPU or the GMCH receives data it monitors DINV[3:0]# to determine if the corresponding data segment should be inverted.

6.2.1 System Bus Interrupt Delivery

The Intel Celeron M processor support system bus interrupt delivery. It does not support the APIC serial bus interrupt delivery mechanism. Interrupt related messages are encoded on the system bus as Interrupt Message transactions. System bus interrupts may originate from the processor on the system bus, or from a downstream device on the Hub interface.

In a GMCH platform, the ICH4-M contains IOxAPICs and its interrupts are generated as upstream Hub interface Memory Writes. Furthermore, PCI 2.2 defines MSI's (Message Signaled Interrupts) that are also in the form of Memory Writes. A PCI 2.2 device may generate an interrupt as an MSI cycle on its PCI bus instead of asserting a hardware signal to the IOxAPIC. The MSI may be directed to the IOxAPIC, which in turn generates an interrupt as an upstream Hub interface memory write. Alternatively the MSI may be directed directly to the system bus. The target of an

MSI is dependent on the address of the interrupt Memory Write. The GMCH forwards inbound Hub interface memory writes to address 0FEEx_xxxxh, to the system bus as Interrupt Message transactions.

6.2.2 Upstream Interrupt Messages

The GMCH accepts message based interrupts from its Hub interface and forwards them to the system bus as Interrupt Message transactions. The Interrupt Messages presented to the GMCH are in the form of Memory Writes to address 0FEEx_xxxxh. At the Hub interface, the Memory Write Interrupt Message is treated like any other Memory Write; it is either posted into the inbound data buffer (if space is available) or retried (if data buffer space is not immediately available). Once posted, the Memory Write from the Hub interface, to address 0FEEx_xxxxh, is decoded as a cycle that needs to be propagated by the GMCH to the front side bus as an Interrupt Message transaction.

6.3 System Memory Interface

6.3.1 DDR SDRAM Interface Overview

The GMCH supports DDR SDRAM at 200/266-MHz and includes the following support:

- Up to 1 GB of PC2100/PC2700 DDR SDRAM
- Maximum of two DDR DIMMs, single-sided and/or double-sided

The 2-bank select lines SBA[1:0] and the 13 Address lines SMA[12:0] allow the GMCH to support 64-bit wide DDR DIMMs using 128-Mb, 256-Mb, and 512-Mb DDR SDRAM technology. While address lines SMA[9:0] determine the starting address for a burst, burst length can only be 4. Four chip selects SCS[3:0]# lines allow a maximum of two rows of single-sided DDR SDRAM DIMMs and four rows of double-sided DDR SDRAM DIMMs.

The GMCH main system memory controller targets CAS latencies of 2 and 2.5 for DDR SDRAM. The GMCH provides refresh functionality with a programmable rate (normal DDR SDRAM rate is 1 refresh/15.6 µs). For write operations of less than a full cache line, GMCH will perform a cache-line read and into the write buffer and perform byte-wise write-merging in the write buffer.

6.3.2 System Memory Organization and Configuration

6.3.2.1 Configuration Mechanism for DDR DIMMs

Detection of the type of DDR SDRAM installed on the DDR DIMM is supported via Serial Presence Detect mechanism as defined in the JEDEC 200-pin DDR DIMM specification.

Before any cycles to the system memory interface can be supported, the GMCH DDR SDRAM registers must be initialized. The GMCH must be configured for operation with the installed system memory types. Detection of system memory type and size is done via the System Management Bus (SMB) interface on the ICH4-M. This two-wire bus is used to extract the DDR SDRAM type and size information from the Serial Presence Detect port on the DDR SDRAM DDR DIMMs. DDR SDRAM DIMMs contain a 5-pin Serial Presence Detect interface, including SCL (serial clock), SDA (serial data) and SA[2:0]. Devices on the SMBus have a 7-bit address. For the DDR SDRAM DIMMs, the upper four bits are fixed at 1010b. The lower three bits are strapped on the SA[2:0] pins. SCL and SDA are connected directly to the System Management bus on the ICH4-M. Thus data is read from the Serial Presence Detect port on the DDR DIMMs via a

series of I/O cycles to the south bridge. The BIOS needs to determine the size and type of system memory used for each of the rows of system memory in order to properly configure the GMCH system memory interface.

For SMBus Configuration and Access of the Serial Presence Detect Ports, refer to the *Intel® 82801DBM I/O Controller Hub 4 (ICH4-M) Datasheet* (252337) for more detail.

6.3.2.2 System Memory Register Programming

This section provides an overview of how the required information for programming the DDR SDRAM registers is obtained from the Serial Presence Detect ports on the DDR DIMMs. The Serial Presence Detect ports are used to determine Refresh Rate, MA and MD Buffer Strength, row Type (on a row by row basis), DDR SDRAM Timings, row sizes and row page sizes. Table 30 lists a subset of the data available through the on board Serial Presence Detect ROM on each DDR DIMM.

Table 30. Data Bytes on DDR DIMM Used for Programming DRAM Registers

Byte	Function
2	System Memory Type (DDR SDRAM)
3	Number of row addresses, not counting Bank Addresses
4	Number of Column Addresses
5	Number of DIMM banks
12	Refresh Rate/Type
17	Number Banks on each Device

Table 30 is only a subset of the defined SPD bytes on the DDR DIMMs. These bytes collectively provide enough data for programming the GMCH DDR SDRAM registers.

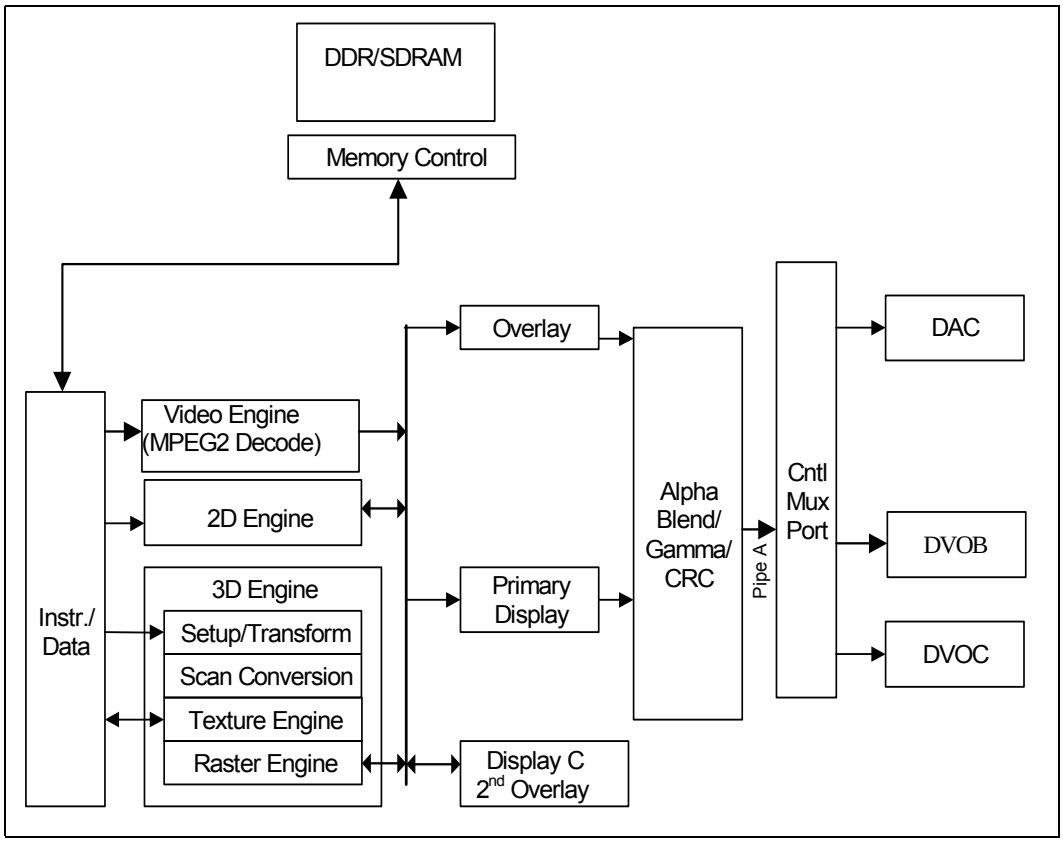
6.3.3 DDR SDRAM Performance Description

The overall system memory performance is controlled by the DDR SDRAM timing register, pipelining depth used in GMCH, system memory speed grade and the type of DDR SDRAM used in the system. Besides this, the exact performance in a system is also dependent on the total system memory supported, external buffering and system memory array layout. The most important contribution to overall performance by the system memory controller is to minimize the latency required to initiate and complete requests to system memory, and to support the highest possible bandwidth (full streaming, quick turn-arounds). One measure of performance is the total flight time to complete a cache line request. A true discussion of performance really involves the entire chipset, not just the system memory controller.

6.4 Integrated Graphics Overview

The Intel® 82854 GMCH provides a highly integrated graphics accelerator and PCI set while allowing a flexible Integrated System Graphics solution.

Figure 7. Intel® 82854 GMCH Graphics Block Diagram (Native Graphic Mode only)



High bandwidth access to data is provided through the system memory port. The GMCH uses a tiling architecture to minimize page miss latencies and thus maximize effective rendering bandwidth.

6.4.1 3D/2D Instruction Processing

The GMCH contains an extensive set of instructions that control various functions including 3D rendering, BLT operations, display, MPEG decode acceleration, and overlay. The 3D instructions set 3D pipeline states and control the processing functions. The 2D instructions provide an efficient method for invoking BLT operations.

6.4.2 3D Engine

The 3D engine of the GMCH has been designed with a deeply pipelined architecture, where performance is maximized by allowing each stage of the pipeline to simultaneously operate on different primitives or portions of the same primitive. The GMCH supports the following:

- Perspective-corrected Texture mapping
- Multitexturing
- Embossed and Dot-Product Bump mapping
- Cubic Environment Maps
- Bilinear, Trilinear, and Anisotropic MIP map filtering
- Gouraud shading and Flat shading
- Alpha-blending
- Per-Vertex and per- pixel fog
- Z/W buffering

These features are independently controlled via a set of 3D instructions. The 3D pipeline subsystem performs the 3D rendering acceleration. The main blocks of the pipeline are the Setup Engine, Scan Converter, Texture Pipeline, and Raster Pipeline. A typical programming sequence would be to send instructions to set the state of the pipeline followed by rendering instructions containing 3D primitive vertex data.

6.4.2.1 Setup Engine

The GMCH 3D setup engine takes the input data associated with each vertex of a 3D primitive and computes the various parameters required for scan conversion. In formatting this data, the GMCH maintains sub-pixel accuracy. The per-vertex data is converted into gradients that can be used to interpolate the data at any pixel within a polygon (colors, alpha, Z or W depth, fog, and texture coordinates). The pixels covered by a polygon are identified and per-pixel texture addresses are calculated.

6.4.2.2 Viewport Transform and Perspective Divide

A 3D-geometry pipeline typically involves transformation of vertices from model space to clipping space followed by clip test and clipping. Lighting can be performed during the transformation or at any other point in the pipeline. After clipping, the next stage involves perspective divide followed by transformation to the viewport or screen space. The GMCH can support viewport transform and perspective divide portion of the 3D geometry pipeline in hardware.

6.4.2.3 3D Primitives and Data Formats Support

The 3D primitives rendered by the GMCH are points, lines, discrete triangles, line strips, triangle strips, triangle fans, and polygons. In addition to this, the GMCH supports DirectX's* Flexible Vertex Format* (FVF), which enables the application to specify a variable length parameter list, obviating the need for sending unused information to the hardware. Strips, Fans, and Indexed Vertices as well as FVF improves delivered vertex rate to the setup engine significantly.

6.4.2.4 Pixel Accurate Fast Scissoring and Clipping Operation

The GMCH supports clipping to a scissoring rectangle within the drawing window. The GMCH clipping and scissoring in hardware reduce the need for software to process polygons, and thus improves performance. During the setup stage, the GMCH clips polygons to the drawing window.

The scissor rectangle accelerates the clipping process by allowing the driver to clip to a bigger region than the hardware renders to. The scissor rectangle is pixel accurate, and independent of line and point width. The GMCH supports a single scissor box rectangle.

6.4.2.5 Backface Culling

As part of the setup, the GMCH can discard polygons from further processing, if they are either facing away from or towards the user's viewpoint. This operation, referred to as Back Face Culling is accomplished based on the clockwise or counter-clockwise orientation of the vertices on a primitive. This can be enabled or disabled by the driver.

6.4.2.6 Scan Converter

The Scan Converter takes the vertex and edge information identifies all pixels that are affected by features being rendered. It works on a per-polygon basis, and one polygon may be entering the pipeline while calculations finish on another.

6.4.2.7 Texture Engine

The GMCH allows an image pattern or video to be placed on the surface of a 3D polygon. The texture engine performs texture color or chromakey matching texture filtering (anisotropic, trilinear, and bilinear) and YUV to RGB conversion.

As texture sizes increase beyond the bounds of graphics memory, executing textures from graphics memory becomes impractical. Every rendering pass would require copying each and every texture in a scene from system memory to graphics memory, then using the texture, and finally overwriting the local memory copy of the texture by copying the next texture into graphics memory. The GMCH, using Intel's Direct Memory Execution model, simplifies this process by rendering each scene using the texture located in system memory. The GMCH includes a cache controller to avoid frequent memory fetches of recently used texture data.

6.4.2.8 Perspective Correct Texture Support

A textured polygon is generated by mapping a 2D texture pattern onto each pixel of the polygon. A texture map is like wallpaper pasted onto the polygon. Since polygons are rendered in perspective, it is important that texture be mapped in perspective as well. Without perspective correction, texture is distorted when an object recedes into the distance. Perspective correction involves a compute-intensive "per-pixel-divide" operation on each pixel. Perspective correction is necessary for realistic 3D graphics.

6.4.2.9 Texture Decompression

As the textures' average size gets larger with higher color depth and multiple textures become the norm, it becomes increasingly important to provide support for compressed textures.

DirectX* supports Texture Compression/Decompression to reduce the bandwidth required to deliver textures. The GMCH supports several compressed texture formats (DirectX: DXT1, DXT2, DXT3, DXT4, DXT5) and OpenGL FXT1 formats.

6.4.2.10 Texture Chromakey

Chromakey is a method for removing a specific color or range of colors from a texture map before it is applied to an object. For nearest texture filter modes, removing a color simply makes those portions of the object transparent (the previous contents of the back buffer show through). For linear texture filtering modes, the texture filter is modified if only the non-nearest neighbor texels match the key (range).

Chromakeying can be performed for both paletted and non-paletted textures, and removes texels that fall within a specified color range. The Chromakey mode refers to testing the ARGB or YUV components to see if they fall between high and low state variable values. If the color of a texel contribution is in this range and chromakey is enabled, then this contribution is removed from the resulting pixel color.

6.4.2.11 Anti-Aliasing

Aliasing is one of the artifacts that degrade image quality. In its simplest manifestation, aliasing causes the jagged staircase effects on sloped lines and polygon edges. Another artifact is the moiré patterns, which occur as a result of the fact that there is very small number of pixels available on screen to contain the data of a high-resolution texture map.

Full scene anti-aliasing uses super-sampling, which means that the image is rendered internally at a higher resolution than it is displayed on screen. The GMCH renders internally at 1600x1200, reads the image as a texture, and finally down-samples (via a Bilinear filter) to the screen resolution of 640x480 and 800x600. Full scene anti-aliasing removes jaggies at the edges.

6.4.2.12 Texture Map Filtering

Many texture-mapping modes are supported. Perspective correct mapping is always performed. As the map is fitted across the polygon, the map can be tiled, mirrored in either the U or V directions, or mapped up to the end of the texture and no longer placed on the object (this is known as clamp mode). The way a texture is combined with other object attributes is also definable.

The GMCH supports up to 12 Levels-of-Detail (LODs) ranging in size from 2048x2048 to 1x1 texels. (A texel is defined as a texture map element.) Included in the texture processor is a texture cache, which provides efficient MIP-mapping.

The GMCH supports seven types of texture filtering:

- Nearest (also known as Point filtering): Texel with coordinates nearest to the desired pixel is used. (This is used if only one LOD is present.)
- Linear (also known as Bilinear filtering): A weighted average of a 2x2 area of texels surrounding the desired pixel is used. (This is used if only one LOD is present.)
- Nearest MIP Nearest (also known as Point filtering): This is used if many LODs are present. The nearest LOD is chosen and the texel with coordinates nearest to the desired pixel are used.
- Linear MIP Nearest (Bilinear MIP mapping): This is used if many LODs are present. The nearest LOD is chosen and a weighted average of a 2x2 area of texels surrounding the desired pixel is used (four texels). This is also referred to as Bilinear MIP Mapping.
- Nearest MIP Linear (Point MIP mapping): This is used if many LODs are present. Two appropriate LODs are selected and within each LOD the texel with coordinates nearest to the desired pixel are selected. The Final texture value is generated by linear interpolation between the two texels selected from each of the MIP Maps.
- Linear MIP Linear (Trilinear MIP mapping): This is used if many LODs are present. Two appropriate LODs are selected and a weighted average of a 2x2 area of texels surrounding the desired pixel in each MIP Map is generated (four texels per MIP Map). The Final texture value is generated by linear interpolation between the two texels generated for each of the MIP

Maps. Trilinear MIP Mapping is used minimize the visibility of LOD transitions across the polygon.

- Anisotropic MIP Nearest (Anisotropic filtering): This filter can be used when textured object pixels map back to significantly non-square regions of the texture (e.g., when the texture is scaled in one screen direction than the other screen direction).

Both DirectX and OpenGL (Rev.1.1) allow support for all these filtering modes.

6.4.2.13 Multiple Texture Composition

The GMCH also performs multiple texture composition. This allows the combination of two or greater MIP maps to produce a new one with new LODs and texture attributes in a single or iterated pass. The setup engine supports up to four texture map coordinates in as single pass. The GMCH allows up to two Bilinear MIP Maps or a single Trilinear MIP Map to be composited in a single pass. Greater than two Bilinear MIP Maps or more than one Trilinear MIP Map would require multiple passes. The actual blending or composition of the MIP Maps is done in the raster engine. The texture engine provides the required texels including blending information.

Flexible vertex format support allows multi-texturing because it makes it possible to pass more than one texture in the vertex structure.

6.4.2.14 Cubic Environment Mapping

Environment maps allow applications to render scenes with complex lighting and reflections while significantly decreasing CPU load. There are several methods to generate environment maps such as spherical, circular and cubic. The GMCH supports cubic reflection mapping over spherical and circular since it is the best choice to provide real-time environment mapping for complex lighting and reflections.

Cubic Mapping supports a texture map for each of the 6 cube faces. These can be generated by pointing a camera with a 90-degree field-of-view in the appropriate direction. Per-vertex vectors (normal, reflection or refraction) are interpolated across the polygon and the intersection of these vectors with the cube texture faces are calculated. Texel values are then read from the intersection point on the appropriate face and filtered accordingly.

6.4.2.15 Bump Mapping

The GMCH only supports embossed and dot product bump mapping, not environment bump mapping.

6.4.3 Raster Engine

The Raster engine is where the color data such as fogging, specular RGB, texture map blending, etc. is processed. The final color of the pixel is calculated and the RGB value is combined with the corresponding components resulting from the Texture engine. These textured pixels are modified by the specular and fog parameters. These specular highlighted, fogged, textured pixels are color blended with the existing values in the frame buffer. In parallel, stencil, alpha, and depth buffer tests are conducted which will determine whether the Frame and Depth buffers will be updated with the new pixel values.

6.4.3.1 Texture Map Blending

Multiple textures can be blended together in an iterative process and applied to a primitive. The GMCH allows up to four distinct or shared texture coordinates and texture maps to be specified onto the same polygon. Also, the GMCH supports a texture coordinate set to access multiple texture maps. State variables in multiple textures are bound to texture coordinates, texture map or texture blending.

6.4.3.2 Combining Intrinsic and Specular Color Components

The GMCH allows an independently specified and interpolated specular RGB attribute to be added to the post-texture blended pixel color. This feature provides a full RGB specular highlight to be applied to a textured surface, permitting a high quality reflective colored lighting effect not available in devices which apply texture after the lighting components have been combined. If the specular-add state variable is disabled, only the resultant colors from the map blending are used. If this state variable is enabled, the specular RGB color is added to the RGB values from the output of the map blending.

6.4.3.3 Color Shading Modes

The Raster engine supports the Flat and Gouraud shading modes. These shading modes are programmed by the appropriate state variables issued through the command stream.

- Flat shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue), Specular (R, G, B), Fog, and Alpha to the pixel, where each vertex color has the same value. The setup engine substitutes one of the vertex's attribute values for the other two vertices attribute values thereby creating the correct flat shading terms. This condition is set up by the appropriate state variables issued prior to rendering the primitive.
- Gouraud shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue). Specular (RGB), Fog, and Alpha to the pixel, where each vertex color has a different value.

6.4.3.4 Color Dithering

Color Dithering in the GMCH helps to hide color quantization errors for 16-bit color buffers. Color Dithering takes advantage of the human eye's propensity to average the colors in a small area. Input color, alpha, and fog components are converted from 8-bit components to 5-bit or 6-bit component by dithering. Dithering is performed on blended textured pixels. In 32-bit mode, dithering is not performed.

6.4.3.5 Vertex and Per Pixel Fogging

Fogging is used to create atmospheric effects such as low visibility conditions in flight simulator-type games. It adds another level of realism to computer-generated scenes. Fog can be used for depth cueing or hiding distant objects. With fog, distant objects can be rendered with fewer details (less polygons), thereby improving the rendering speed or frame rate. Fog is simulated by attenuating the color of an object with the fog color as a function of distance, and the greater the distance, the higher the density (lower visibility for distant objects). There are two ways to implement the fogging technique: per-vertex (linear) fogging and per-pixel (non-linear) fogging. The per-vertex method interpolates the fog value at the vertices of a polygon to determine the fog factor at each pixel within the polygon. This method provides realistic fogging as long as the polygons are small. With large polygons (such as a ground plane depicting an airport runway), the per-vertex technique results in unnatural fogging.

The GMCH supports both types of fog operations, vertex and per pixel. If fog is disabled, the incoming color intensities are passed unchanged to the destination blend unit. If fog is enabled, the incoming pixel color is blended with the fog color based on a fog coefficient on a per pixel basis.

6.4.3.6 Alpha Blending

Alpha blending in the GMCH adds the material property of transparency or opacity to an object. Alpha blending combines a source pixel color and alpha component with a destination pixel color and alpha component. For example, this is so that a glass surface on top (source) of a red surface (destination) would allow much of the red base color to show through.

Blending allows the source and destination color values to be multiplied by programmable factors and then combined via a programmable blend function. The combined and independent selection of factors and blend functions for color and alpha is supported.

6.4.3.7 Color Buffer Formats: (Destination Alpha)

The Raster engine supports 8-bit, 16-bit, and 32-bit Color Buffer formats. The 8-bit format is used to support planar YUV4:2:0 format, which is used only in Motion Compensation and Arithmetic Stretch format. The bit format of Color and Z is allowed to mix.

The GMCH can support an 8-bit destination alpha in 32-bit mode. Destination alpha is supported in 16-bit mode in 1:5:5:5 or 4:4:4:4 format. The GMCH does not support general 3D rendering to 8-bit surfaces. 8-bit destinations are supported for operations on planar YUV surfaces (for example, stretch BLTs) where each 8-bit color component is written in a separate pass. The GMCH also supports a mode where both U and V planar surfaces can be operated on simultaneously.

The frame buffer of the GMCH contains at least two hardware buffers - the Front Buffer (display buffer) and the Back Buffer (rendering buffer). While the back buffer may actually coincide with (or be part of) the visible display surface, a separate (screen or window-sized) back buffer is typically used to permit double-buffered drawing. That is, the image being drawn is not visible until the scene is complete and the back buffer made visible or copied to the front buffer via a 2D BLT operation. Rendering to one buffer and displaying from the other buffer removes image tearing artifacts. Additionally, more than two back buffers (for example, triple-buffering) can be supported.

6.4.3.8 Depth Buffer

The Raster Engine is able to read and write from this buffer and use the data in per fragment operations that determine resultant color and depth value of the pixel for the fragment are to be updated or not.

Typical applications for entertainment or visual simulations with exterior scenes require far/near ratios of 1000 to 10000. At 1000, 98% of the range is spent on the first 2% of the depth. This can cause hidden surface artifacts in distant objects, especially when using 16-bit depth buffers. A 24-bit Z-buffer provides 16 million Z-values as opposed to only 64 k with a 16-bit Z-buffer. With lower Z-resolution, two distant overlapping objects may be assigned the same Z-value. As a result, the rendering hardware may have a problem resolving the order of the objects, and the object in the back may appear through the object in the front.

By contrast, when w (or eye-relative z) is used, the buffer bits can be more evenly allocated between the near and far clip planes in world space. The key benefit is that the ratio of far and near is no longer an issue, and allows applications to support a maximum range of miles, yet still get

reasonably accurate depth buffering within inches of the eye point. The selection of depth buffer size is relatively independent of the color buffer. A 16-bit Z/W or 24-bit Z/W buffer can be selected with a 16-bit color buffer. Z buffer is not supported in 8-bit mode.

6.4.3.9 Stencil Buffer

The Raster engine provides 8-bit stencil buffer storage in 32-bit mode and the ability to perform stencil testing. Stencil testing controls 3D drawing on a per pixel basis and conditionally eliminates a pixel on the outcome of a comparison between a stencil reference value and the value in the stencil buffer at the location of the source pixel being processed. They are typically used in multipass algorithms to achieve special effects, such as decals, outlining, shadows, and constructive solid geometry rendering.

One of three possible stencil operations is performed when stencil testing is enabled. The stencil operation specifies how the stencil buffer is modified when a fragment passes or fails the stencil test. The selection of the stencil operation to be performed is based upon the result of the stencil test and the depth test. A stencil write mask is also included that controls the writing of particular bits into the stencil buffer. It selects between the destination value and the updated value on a per-bit basis. The mask is 8-bit wide.

6.4.3.10 Projective Textures

The GMCH supports two simultaneous projective textures at full rate processing. These textures require three floating-point texture coordinates to be included in the FVF format. Projective textures enable special effects such as projecting spot light textures obliquely onto walls, and so on.

6.4.4 2D Engine

The GMCH provides an extensive set of 2D instructions and 2D HW acceleration for block transfers of data (BLTs). The BLT engine provides the ability to copy a source block of data to a destination and perform operations (for example, ROP1, ROP2, and ROP3) on the data using a pattern, and/or another destination. The Stretch BLT engine is used to move source data to a destination that need not be the same size, with source transparency. Performing these common tasks in hardware reduces CPU load, and thus improves performance.

6.4.4.1 256-Bit Pattern Fill and BLT Engine

Use of this BLT engine accelerates the Graphical User Interface (GUI) of Microsoft* Windows*. The GMCH BLT Engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The term BLT refers to a block transfer of pixel data between system memory locations. The BLT engine can be used for the following:

- Move rectangular blocks of data between system memory locations
- Data alignment
- Perform logical operations (raster ops)

The rectangular block of data does not change as it is transferred between system memory locations. Data to be transferred can consist of regions of system memory, patterns, or solid color fills. A pattern will always be 8x8 pixels wide and may be 8-bits, 16-bits, or 32-bits per pixel.

The GMCH BLT engine has the ability to expand monochrome data into a color depth of 8 bits, 16 bits, or 32 bits. BLTs can be either opaque or transparent. Opaque transfers, move the data specified to the destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source system memory location, the GMCH can specify which area in system memory to begin the BLT transfer. Hardware is included for all 256 raster operations (source, pattern, and destination) defined by Microsoft, including transparent BLT.

The GMCH has instructions to invoke BLT operations, permitting software to set up instruction buffers and use batch processing as described in the Instruction Processing section. The GMCH can perform hardware clipping during BLTs.

6.4.4.2 Alpha Stretch BLT

The stretch BLT function can stretch source data in the X and Y directions to a destination larger or smaller than the source. Stretch BLT functionality expands a region of system memory into a larger or smaller region using replication and interpolation. The stretch BLT function also provides format conversion and data alignment.

6.4.5 Planes and Engines

The GMCH display can be functionally delineated into planes and engines (pipes and ports). A plane consists of rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces, which are rectangular system memory surfaces with a similar set of characteristics. They are also associated with a particular destination pipe.

A pipe consists of a set of planes that will be combined with a timing generator. A port is the destination for the result of the pipe. The GMCH supports one Analog Output Port and two DVO ports. In conclusion, planes are associated with pipes and pipes are associated with ports.

6.4.5.1 Dual Pipe Independent Display Functionality (Native Graphic Mode only)

The display consists of two display pipes, A and B. Pipes have a set of planes that are assigned to them as sources. The analog display port may only use Pipe A or Pipe B, the DVO B or C ports may use either Pipe A or Pipe B. This limits the resolutions available on a digital display when an analog CRT is active.

Table 31. Dual Display Usage Model (Native Graphic Mode only)

Display Pipe A	Display Pipe B
DVO B or C or Both	CRT
CRT	DVO B or C or Both
DVO B	DVO C

6.4.6 Hardware Cursor Plane (Native Graphic Mode only)

The GMCH supports two hardware cursors. The cursor plane is one of the simplest display planes. With a few exceptions, has a fixed size of 64 x 64 and a fixed Z-order (top). In legacy modes, cursor can cause the display data below it to be inverted. In the alpha blend mode, true color cursor data can be alpha blended into the display stream. It can be assigned to either display pipe A or display pipe B and dynamically flipped from one to the other when both are running.

6.4.6.1 Cursor Color Formats

Color data can be in an indexed format or a true color format. Indexed data uses the entries in the four-entry cursor palette to convert the two-bit index to a true color format before being passed to the blenders. The index can optionally specify that a cursor pixel be transparent or cause an inversion of the pixel value below it or one of two colors from the cursor palette. Blending of YUV or RGB data is only supported with planes that have data of the same format.

6.4.6.2 Popup Plane (Second Cursor)

The popup plane is used for control functions in mobile applications. Only the hardware cursor has a higher Z-order precedence over the hardware icon. In standard modes (non-VGA) either cursor A or cursor B can be used as a Popup Icon. For VGA modes, 32-bpp data format is not supported.

6.4.6.3 Popup Color Formats

Source color data for the popup is in an indexed format. Indexed data uses the entries in the four-entry cursor palette to convert the two-bit index to a true color format before being passed to the blenders. Blending of color data is only supported with data of the same format.

6.4.7 Overlay Plane

The overlay engine provides a method of merging either video capture data (from an external Video Capture device) or data delivered by the CPU, with the graphics data on the screen.

6.4.7.1 Multiple Overlays (Display C)

A single overlay plane and scalar is implemented. This overlay plane can be connected to the primary display, secondary display or in bypass mode. In the default mode, it appears on the primary display. The overlay may be displayed in a multi-monitor scenario for single-pipe simultaneous displays only. Picture-in-Picture feature is supported via software through the arithmetic stretch BLT.

6.4.7.2 Source/Destination Color/Chromakeying

Overlay source/destination chromakeying enables blending of the overlay with the underlying graphics background. Destination color-/chromakeying can be used to handle occluded portions of the overlay window on a pixel-by-pixel basis that is actually an underlay. Destination color keying supports a specific color (8-bit or 15-bit) mode as well as 32-bit alpha blending.

Source color/chromakeying is used to handle transparency based on the overlay window on a pixel-by-pixel basis. This is used when "blue screening" an image to overlay the image on a new background later.

6.4.7.3 Gamma Correction

To compensate for overlay color intensity loss, the overlay engine supports independent gamma correction. This allows the overlay data to be converted to linear data or corrected for the display device when not blending.

6.4.7.4 YUV to RGB Conversion

The format conversion can be bypassed in the case of RGB source data.

6.4.7.5 Color Control

Color control provides a method of changing the color characteristics of the pixel data. It is applied to the data while in YUV format and uses input parameters such as brightness, saturation, hue (tint) and contrast. This feature is supplied for the overlay only and works in YUV formats only.

6.4.7.6 Dynamic Bob and Weave

Interlaced data that originates from a video camera creates two fields that are temporally offset by 1/60 of a second. There are several schemes to de-interlace the video stream: line replication, vertical filtering, field merging, and vertical temporal filtering. Field merging takes lines from the previous field and inserts them into the current field to construct the frame - this is known as weaving. This is the best solution for images with little motion; however, showing a frame that consists of the two fields will have serration or feathering of moving edges when there is motion in the scene. Vertical filtering or "Bob" interpolates adjacent lines rather replicating the nearest neighbor. This is the best solution for images with motion however, it will have reduced spatial resolution in areas that have no motion and introduce jaggies. In absence of any other de-interlacing, these form the baseline and are supported by the GMCH.

6.4.8 Video Functionality

The GMCH supports MPEG-2 decoding hardware, sub-picture support and DTV.

6.4.8.1 MPEG-2 Decoding

The GMCH MPEG2 Decoding supports Hardware Motion Compensation (HWMC). The GMCH can accelerate video decoding for the following video coding standards:

- MPEG-2 support
- MPEG-1: Full feature support
- H.263 support
- MPEG-4: Only supports some features in the simple profile

The HWMC interface supports Hardware Video Acceleration Compatible API's (HVA).

6.4.8.2 Hardware Motion Compensation

The HWMC process consists of reconstructing a new picture by predicting (either forward, backward, or bi-directional) the resulting pixel colors from one or more reference pictures. The GMCH receives the video stream and implements Motion Compensation and subsequent steps in hardware. Performing Motion Compensation in hardware reduces the processor demand of software-based MPEG-2 decoding, and thus improves system performance.

6.4.8.3 Sub-picture Support

Sub-picture is used for two purposes: Subtitles for movie captions, which are superimposed on a main picture, and for menus to provide some visual operation environments for the user.

DVD allows movie subtitles to be recorded as sub-pictures. On a DVD disc, it is called subtitle because it has been prepared for storing captions. Since the disc can have a maximum of 32 tracks for subtitles, they can be used for various applications, for example, as Subtitles in different languages.

There are two kinds of menus, the System menus and other In-Title menus. First, the System menus are displayed and operated at startup of or during the playback of the disc or from the stop state. Second, In-Title menus can be programmed as a combination of Sub-picture and Highlight commands to be displayed during playback of the disc.

The GMCH supports sub-picture for DVD by mixing the two video streams via alpha blending. Unlike color keying, alpha blending provides a softer effect and each pixel that is displayed is a composite between the two video stream pixels. The GMCH can utilize four methods when dealing with sub-pictures. This flexibility means that the GMCH can work with all sub-picture formats.

6.5 Internal Graphic Display Interface

The GMCH has three dedicated display ports: an Analog CRT port and two Digital display ports, DVOB and DVOC.

When the GMCH is strapped to operate in Native Graphic Mode, the DVOB and DVOC can support down stream devices such as TV-out encoders, external DACs, LVDS transmitters, and TMDS transmitters. Each display port has control signals that may be used to control, configure and/or determine the capabilities of an external device. The data that is sent out the display ports are selected from one of the two possible sources, display pipe A or display pipe B.

The GMCH's digital display port is capable of driving a 165-MHz pixel clock on a single DVO port, or a 330-MHz pixel clock by combining DVOB and DVOC.

6.5.1 Pipe A Timing Generator Unit

The Pipe A Timing generator provides the basic timing information for Display Pipe A. Timings are composed of blank, sync, border and active periods. The active period represents the data area; this is normally the size of a fixed resolution display or the selected resolution. Sync happens only within blank periods thereby dividing the blank into three regions consisting of a front porch, sync time, and back porch. Borders only happen directly before the start of blank and directly after the end of blank. Borders are referred to as left, right, top, or bottom. The Pipe A timing generator has been adapted to offer interlace support for the generation of HSYNC and VSYNC relative timing to support downstream field identification. It has also been adapted to provide interlace timing support for 480i and PAL formats. The following sections detail the features supported by the Intel® 82854 GMCH.

6.5.1.1 ARIB Support

Please refer to the ARIB TR-B15 Operational Guidelines for Digital Satellite Broadcasting (detailed Implementation guideline for receiver) for an exhaustive coverage of this topic (http://www.arib.or.jp/english/html/overview/ov/tr_b15.html). The Intel® 82854 GMCH supports the ARIB resolutions in Figure 8 except the Motion Picture (Movie) Plane and the Movie/Still picture selection plane. This device supports the remaining planes outlined in Figure 8.

Figure 8. ARIB TR-B15 Plane Resolutions

Plane name	Requirements	
Still Picture Plane	Resolution	1920x1080x16, YCbCr(4:2:2), 16:9
		720x480x16, YCbCr(4:2:2), 16:9
		720x480x16, YCbCr(4:2:2), 4:3
Text and Graphic Plane	Resolution	960x540x8, 16:9 (Display resolution is 1920x1080 – 1 pixel on the plane is transferred to 2x2 pixel on display)
		720x480x8, 16:9
		720x480x8, 4:3
	CLUT	Number of CLUTs: 1 Standard fixed color: 128 colors Receiver dependent color: 32 colors Vender dependent color: 96 colors
	Translation	8 bit index of CLUT input is tranfered to YCbCr (4:2:2) and 4 bit alpha value
Superimpose text plane	Resolution	960x540x8, 16:9 (Display resolution is 1920x1080 – 1 pixel on the plane is transferred to 2x2 pixel on display)
		720x480x8, 16:9
		720x480x8, 4:3
	CLUT	Number of CLUTs: 1 Standard fixed color: 128 colors Receiver dependent color: 32 colors Vender dependent color: 96 colors
	Translation	8 bit index of CLUT input is tranfered to YCbCr (4:2:2) and 4 bit alpha value

6.5.1.2 H, V timing signals for active and blank timing

Figure 9 depicts the major resolutions supported by the Intel® 82854 GMCH, included in this table is support for NTSC and High Definition.

The progressive timing modes are supported by the Intel® 82854 GMCH in Native Graphic Mode.

Figure 9. H, V Parameters

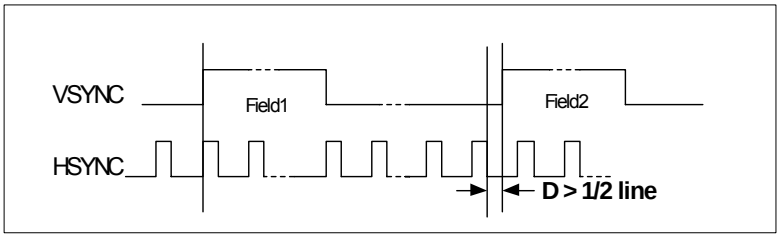
Parameter	480i		480p		720p	1080i	1080p	576i	768p	
Total Vertical Lines	525	525	525	525	750	1125	1125	625	802	805
Active Vertical Lines	480	480	480	480	720	1080	1080	576	768	768
Total Blank Lines	45	45	45	45	30	45	45	49	34	37
Active Line Number	0-239 263-502	0-239 263-502	0-479	0-479	0-719	0-539 563-1102	0-1079	0-287 313-600	0-767	0-767
Total Pixels per Line	858	858	858	858	1650	2200	2200	864	1688	1656
Active Pixels per Line	720	640	720	640	1280	1920	1920	720	1280	1366
Blank Pixels per Line	138	218	138	218	370	280	280	144	408	290
Pixel Clock [MHz]	13.5	13.5	27	27	74.25	74.25	148.5	13.5	81.23	79.99

6.5.1.3 HSYNC/VSYNC Field Timing

The interlace timing is provided on the timing generator associated with Display Pipe A. When data is being driven out of the device, HSYNC and VSYNC accompanies or frames the data. Interlace timing requires that frame data is sent as two fields. Field1 data is scanned out first followed by Field2. The Pipe A timing produces a field timing signal (Field1) that is used by the Video Overlay and Display Plane A to produce Field1/Field2 data.

Downstream devices use the relative placement of the VSYNC and HSYNC timing signals to discern field timing. For Field1 detection, the rising (asserting) edge of VSYNC is coincident with the rising (asserting) edge of HSYNC. For Field2 detection, VSYNC is asserted after the HSYNC pulse and occurs after at least 50% of the line is completed (see Figure 10).

Figure 10. Interlaced Timing Using HSYNC and VSYNC for Field1/Field2 Downstream Detection



Following conditions should be met for the sync (HSYNC, VSYNC) and blank (HBLANK, VBLANK) signals:

- Start of H(V)SYNC can not coincide with start of H(V)BLANK
- H(V)SYNC should always start after H(V)BLANK starts.

In interlaced mode, the Vertical Total (VTOTAL_A register bits 27:16), Vertical Blank End (VBLANK_A register bits 27:16), Vertical Sync Start (VSYNC_A register bits 11:0) and Vertical Sync End (VSYNC_A register bits 27:16) must be programmed to a value 1 less than that of progressive case, which is described in Section 4.5. For example, for VBLANK end at line 525, program the register (VBLANK_A register bits 27:16) as 523 (note that it is 524 for progressive case). This is needed as the line counter is stalled for one line when the Vsync assertion is shifted between field1 and field2.

6.5.2 Blend Function

The blending unit is responsible for combining display planes onto a display pipe. This is done using an alpha blending technique that is described as "pre-multiplied source over destination" or a simple mux operation.

6.5.3 Interlaced Video Field display

The Intel® 82854 GMCH provides interlace timing support for only Plane A and the Video Overlay window. Interlace timing is not available for Plane B, Plane C, Hardware Cursor A, Hardware Cursor B and the VGA plane. The Pipe A timing generator provides the interlace timing for Plane A and the Video Overlay.

6.5.3.1 Interlace support for Plane A graphics

In the Intel® 82854 GMCH, all the graphic features in Native Graphic mode are supported in Plane A, under progressive mode.

In interlace mode, support for Field1 and Field2 timing generation is supported by Plane A. Plane A makes use of the DPODPfieldID signal generated by the Pipe A timing generator to synchronize the field timing. This signal is used to indicate which field of the picture should be scanned out. When DPODPfieldID is high, Field1 is scanned out. The DPODPfieldID is used to set the vertical line counters to the first line. The counters then increment by two until the end of the field is reached. During the VBI interval, the DPODPfieldID transitions to low indicating that Field2 is being processed next. This sets the vertical line counters to the second line and Field2 is then scanned out.

6.5.3.2 ARIB 960 X 540 support

In order to support the conversion of a 960x540 or a 960x1080 Plane A buffer to 1920x1080i, the GMCH supports pixel doubling in the horizontal direction and field replication in the vertical direction. In order to activate this functionality, interlace mode bit 20 in the DVOC- Digital Display Port C Register must be programmed to a 1. Register DSPACNTR-Display A Plane Control Register bits 21:20 are used to program the pixel doubling functionality. The following depicts the bit programming:

00 - No pixel/line multiplication

01 - Pixel AND Line doubling (not valid in interlaced mode)

10 - Reserved

11 - Pixel doubling ONLY (not validated in Native Graphic Mode)

The Field replication mode is used to create two fields of data from Plane A. This is accomplished by scanning out Plane A once to produce Field1 and then rescanned out to produce Field2. In normal interlaced mode, the DSPABASE Register is programmed to the frame buffer start address, the DSPASTER Register is programmed with the frame buffer start address plus one line, and the DSPASTRIDE Register is programmed to 2x the line increment of the image in the frame buffer. For Field1, the DSPABASE and DSPASTRIDE Registers generate addresses into the frame buffer for even lines of the image. For Field2, the DSPASTER and DSPASTRIDE Registers generate addresses into the frame buffer to read odd lines of the image. In field replication mode, the DSPABASE and DSPASTER Registers are programmed with the same start address of the image in the frame buffer. The DSPASTRIDE register is programmed to the 1x line-to-line increment value. With interlaced mode enabled, this will effectively scan out the identical frame buffer for both Field1 and Field2.

Please note that programming bits 21:20 of the DSPACNTR Register to "01" while the interlaced mode is enabled is illegal. In other words, Line doubling is undefined for the interlaced mode of operation.

In order to archieve this, program the PLL to generate Dpclk/2 internally when the following bits of the DSPACNTR-Display A Plane Control Register, bit 21:20, are programmed for pixel duplication mode.

6.5.4 Interlace support for Video Overlay Window

In interlace mode, support for Field1 and Field2 timing generation is supported by the Video Overlay. The Video Overlay makes use of the DPODPfieldID signal generated by the Pipe A timing generator to synchronize the field timing. This signal is used to indicate which field should be scanned out. The Video Overlay determines the correct lines to be used to assemble Field1 and Field2 during on the fly up and down scaling. The Bob method is used to generate the missing field information for Field2 when an interlaced source is used.

Table 32. DVO Control Data Bits

After rising edge of VSYNC	1st pixel clock	2nd pixel clock
DVOB [23]	Buffer ID	Buffer ID
DVOB [22:12]	Undefined	Horizontal image size
DVOB [10:0]	Undefined	Vertical image size

The Display Pipe A timing registers:

HTOTAL_A HBLANK_A HSYNC_A VTOTAL_A

VBLANK_A VSYNC_A PIPEASRC

will hold data associated with physical buffer 0.

The Display Pipe B timing registers:

HTOTAL_B HBLANK_B HSYNC_B VTOTAL_B

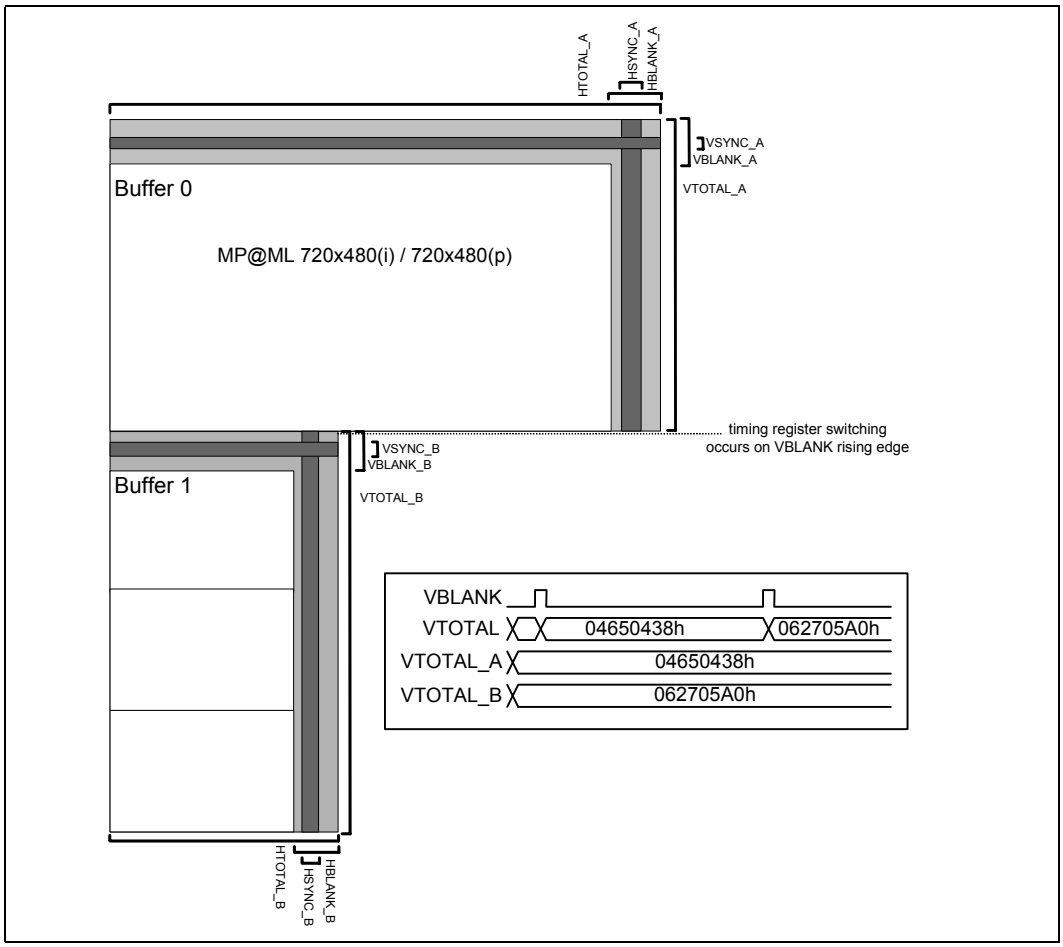
VBLANK_B VSYNC_B PIPEBSRC

will hold data associated with physical buffer 1.

The start address of physical buffer 0 will be in DSPABASE and the start address of physical buffer 1 will be in DSPASEC. The stride for both buffers will be in DSPASTRIDE. Refer to Section 4.0, “Register Description” on page 41 for programming details.

Figure 11 shows how the timing registers switch while the buffer 0 and buffer 1 are scanned out.

Figure 11. Timing Register Switching



As shown in the above figure, buffer switching in Multi-display mode occurs on VBLANK. Once VBLANK is detected, horizontal and vertical counters are reset and register switching occurs. These operations result in an extended HSYNC following the VBLANK. The HSYNC interval following VBLANK rising edge in MTV mode can be calculated as follows:

When switching from Buffer0 to Buffer1:

HSYNC INTERVAL = HSYNC_B[27:16] + 8

When switching from Buffer1 to Buffer0:

HSYNC INTERVAL = HSYNC_A[27:16] + 8

Where HSYNC_A[27:16] and HSYNC_B[27:16] are the Horizontal Sync End values programmed in the PipeA and PipeB Horizontal Sync Registers.

In addition, VBLANK is effectively started twice as a result of the counter reset. This results in two lines of inactive data being repeated. VSYNC will start two lines later then the programmed value, and the total number of lines is extended by two.

6.5.5 Analog Display Port Characteristics

The Analog display port provides an RGB signal output along with an HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT based monitor with a VGA connector.

6.5.5.1 Integrated RAMDAC

The display function contains a 350-MHz, integrated, 24-bit, RAM-based Digital-to-Analog Converter (RAMDAC) that transforms up to 2048X1536 digital pixels at a maximum refresh rate of 75-Hz. Three, 8-bit DACs provide the R, G, and B signals to the monitor.

6.5.5.2 DDC (Display Data Channel)

DDC is defined by VESA. It allows communication between the host system and display. Both configuration and control information can be exchanged allowing plug-and-play systems to be realized. Support for DDC 1 and 2 is implemented.

7.0 Power and Thermal Management

The Intel® 82854 GMCH is intended to be compliant with the following specifications and technologies:

- APM Rev 1.2
- PCI Power Management Rev 1.0
- PC'99, Rev 1.0, PC'99A, and PC'01, Rev 1.0
- ACPI 1.0b and 2.0 support
- ACPI S0, S1-M, S3, S4, S5, C0, C1, C2, C3 states
- Internal Graphics Adapter D0, D1, D3 (Hot/Cold)
- On Die Thermal sensor, enabling core and system memory Write Thermal throttling for prevention of catastrophic thermal conditions
- External Thermal sensor input pin
- Enabling DDR DIMM Thermal throttling
- The GMCH also reduces I/O power dynamically, by disabling sense amps on input buffers, as well as tristating output buffers when possible
- Dynamic Clock Power Down reduces power in all modes of operation
- System memory Self-Refresh in C3 state
- The Intel® 82854 GMCH reduces I/O power dynamically by disabling sense amps on the input buffers, as well as tri-stating the output buffers when possible

7.1 General Description of Supported CPU States

C0 (Full On): This is the only state that runs software. All clocks are running, STPCLK is deasserted, and the processor core is active. The processor can service snoops and maintain cache coherency in this state.

C1 (Auto Halt): The first level of power reduction occurs when the processor executes an Auto-Halt instruction. This stops the execution of the instruction stream and reduces the processor's power consumption. The processor can service snoops and maintain cache coherency in this state.

C2 (Stop Grant): To enter this low power state, STPCLK is asserted. The processor can still service snoops and maintain cache coherency in this state.

C3 (Sleep or Deep Sleep): In these states the processor clock is stopped. The GMCH assumes that no Hub interface cycles (except special cycles) will occur while the GMCH is in this state. The processor cannot snoop its caches to maintain coherency while in the C3 state. The GMCH will transition from the C0 state to the C3 state when software reads the Level 3 Register. This is an ACPI defined register but BIOS or APM (via BIOS) can use this facility when entering a low power state. The Host Clock PLL within the GMCH can be programmed to be shut off for increased power savings and the GMCH uses the DPSLP signal input for this purpose.

C4 (Deeper Sleep): The C4 state appears to the GMCH as identical to the C3 state, but in this state the processor core voltage is lowered. There are no internal events in GMCH for the C4 state that differ from the C3 state. (The C4 state is not supported by the Intel Celeron M Processor, or Genuine Intel Processor).

7.2 General Description of ACPI States

Internal Graphics Adapter:

- D0 Full on, display active
- D1 Low power state, low latency recovery. No display, system memory retained
- D3 Hot - All state lost other than PCI config. system memory lost (optionally)
- D3 Cold - Power off

CPU:

- C0 Full On
- C1 Auto Halt
- C2 Stop Clock. Clk to CPU still running. Clock stopped to CPU core.
- C3 Deep Sleep. Clock to CPU stopped.
- C4 Deeper Sleep. Same as C3 with reduced voltage on the CPU.

System States:

- G0/S0 Full On
- G1/S1-MPower On Suspend (POS). System Context Preserved
- G1/S2Not supported.
- G1/S3Suspend to RAM (STR). Power and context lost to chipset.
- G1/S4Suspend to Disk (STD). All power lost (except wakeup on ICH4-M)
- G2/S5Soft off. Total reboot.

7.3 Internal Thermal Sensor

This section describes the new on-die Thermal sensor capability.

7.3.1 Overview

The Thermal sensor functions are provided below:

Catastrophic Trip Point: This trip point is programmed through the BIOS during initialization. This trip point is set at the temperature at which the GMCH should be shut down immediately with minimal software support. The settings for this are lockable.

High Temperature Trip Point: This trip point is nominally 14ºC below the Catastrophic trip point. The BIOS can be programmed to provide an interrupt when it is crossed in either direction. Upon the trip event, Hardware Throttling may be enabled when the temperature is exceeded.

7.3.2 Hysteresis Operation

Hysteresis provides a small amount of positive feedback to the Thermal sensor circuit to prevent a trip point from flipping back and forth rapidly when the temperature is right at the trip point.

7.4 External Thermal Sensor Input

An External Thermal sensor with a serial interface may be placed next to DDR SDRAM DIMM (or any other appropriate platform location), or a remote Thermal Diode may be placed next to the DDR DIMM (or any other appropriate platform location) and connected to the External Thermal sensor. Intel advises that the External Thermal sensor contains some form of hysteresis, since none is provided by the GMCH hardware.

The external sensor can be connected to the ICH4-M via the SMBus interface to allow programming and setup by BIOS software over the serial interface. The External sensor's output should include an Active-Low Open-Drain signal indicating an Over-Temp condition, which remains asserted for as long as the Over-Temp Condition exists, and deasserts when temperature has returned to within normal operating range. This External sensor output will be connected to the GMCH input (EXTTS_0) and will trigger a Preset Interrupt and/or Read-Throttle on a level-sensitive basis.

Additional External Thermal sensor's outputs, for multiple sensors, can be wire-OR'ed together allow signaling from multiple sensors located physically separately. Software can, if necessary, distinguish which DDR DIMM(s) is the source of the over-temp through the serial interface. However, since the DDR DIMM(s) will be located on the same System Memory Bus Data lines, any GMCH-based Read Throttle will apply equally.

Note: The use of external sensors that include an internal pull-up resistor on the open-drain Thermal trip output is discouraged. However, it may be possible depending on the size of the pull-up and the voltage of the sensor. Please refer to the *Intel® 854 Chipset Platform Design Guide For Use with Ultra Low Voltage Intel® Celeron® M Processor at 600 MHz* (contact your Intel representative for the latest version of this document).

7.4.1 Usage

External sensor(s) used for dynamic temperature feedback control:

- Sensor on DDR DIMMs, which can be used to dynamically control read throttling.

8.0 Intel® 82854 GMCH Strap Pins

8.1 Strapping Configuration

Table 33. Strapping Signals and Configuration

Pin Name	Strap Description	Configuration	I/F Type	Buffer Type
ADDID[0]	Native Graphic Mode select	ADDID[0] = 0, Reserved ADDID[0] = 1, the Intel® 82854 GMCH is strapped to operate under Native Graphic Mode	DVO	IN
HSYNC	XOR Chain Test	Low = Normal Ops (Default) High = XOR Test On	GPIO	OUT
VSYNC	ALL Z Test	Low = Normal Ops (Default) High = AllZ Test On	GPIO	OUT
LCLKCTLB	VTT Voltage Select	Low = Default High = Reserved	GPIO	OUT
DVODETECT	*DVO Select (If DVODETECT=0 during Reset, ADDID[7:0] is latched to the ADDID Register)	Low = DVO (Default) High = Reserved	DVO	BI
GST[2]	* Clock Config: Bit_2	Please refer to Device #0 Function #3 (HPLLCC Register) for proper GST[2:0] settings Please refer to Table 34 for detail configurations on Intel 854 Straps for Frequency/CPU	DVO	Out: 0) Before CPURST#, there is an internal pull-down 1) Just out of CPURST#: These pins are Hi-Z 2) C3: these pins are Hi-Z 3) S1-M: these pins are Hi-Z 4) Internal GFX D1/D3: these pins are Hi-Z 5) S3: these pins are Power down 6) S4/S5: these pins are Power down
GST[1]	* Clock Config: Bit_1			
GST[0]	* Clock Config: Bit_0			
*	Please refer to Device #0 Function #2 (ADD_ID – ADD Identification Register) for proper Native Graphic Mode settings.			
	External pull-ups/downs will be required on the board to enable the non-default state of the straps.			

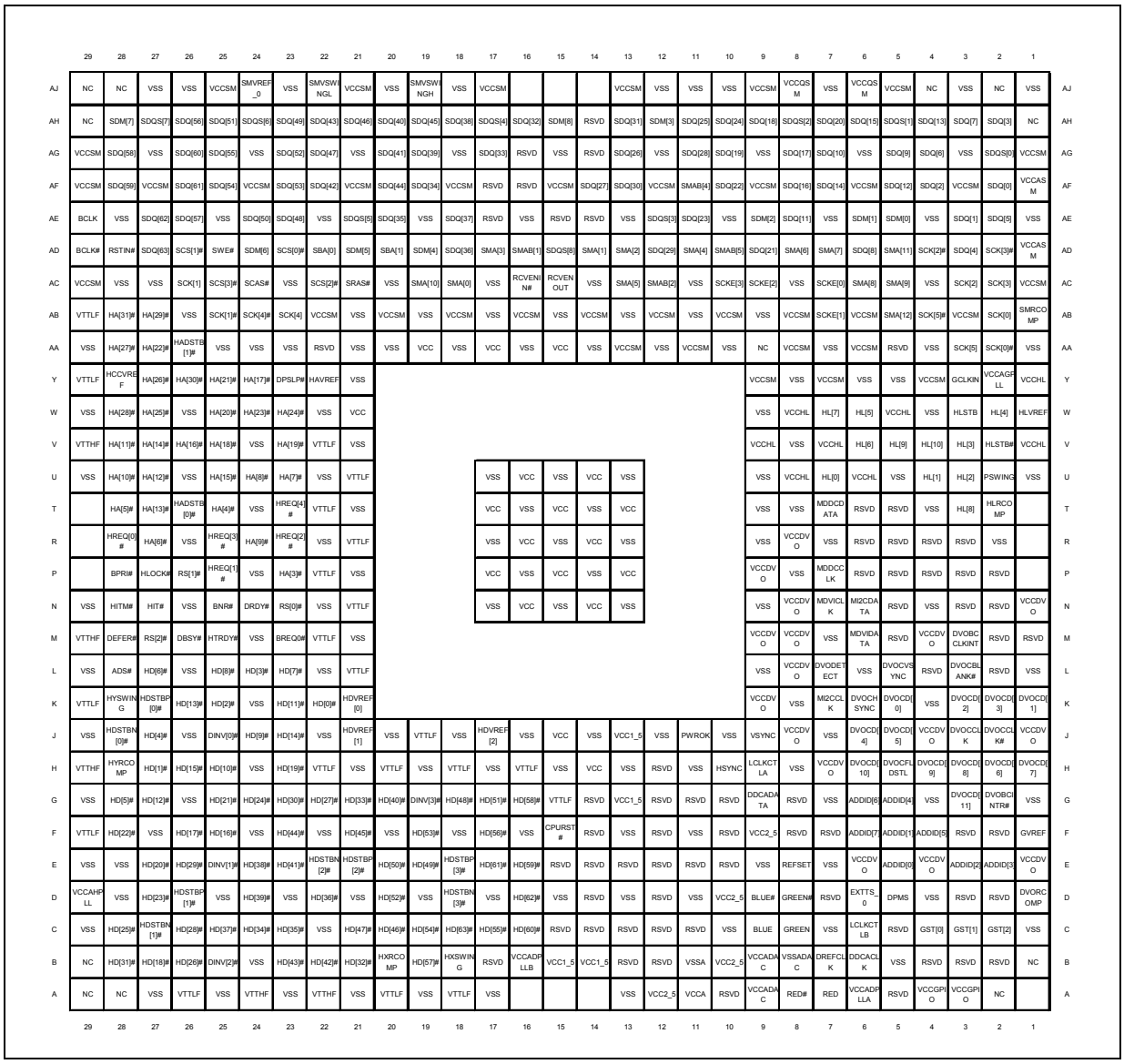
Note: All strap signals are sampled with respect to the leading edge of the Intel® 82854 GMCH PWROK In signal.

Table 34. Intel® 82854 GMCH Straps for Frequency/CPU Configuration

GST[2:0]	LCLKCTLB	CPU	FSB Freq	DDR Freq	Gfx Freq	Core Vcc
000	0	Intel Celeron M Processor Family, Genuine Intel Processor	400MHz	266MHz	200MHz	1.5V
111	0	Intel Celeron M Processor Family, Genuine Intel Processor	400MHz	333MHz	250MHz	1.5V

9.0 Ballout and Package Information

Figure 12. Intel® 82854 GMCH Ballout Diagram (Top View)



	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
AJ	NC	NC	VSS	VSS	VCCSM	SMVREF_0	VSS	SMVSWNGL	VCCSM	VSS	SMVSWNGH	VSS	VCCSM				VCCSM	VSS	VSS	VSS	VCCSM	VCCQSM	VSS	VCCQSM	VCCSM	NC	VSS	NC	VSS	AJ
AH	NC	SDM[7]	SDQS[7]	SDQ[56]	SDQ[51]	SDQS[6]	SDQ[49]	SDQ[43]	SDQ[46]	SDQ[40]	SDQ[45]	SDQ[38]	SDQS[4]	SDQ[32]	SDM[8]	RSVD	SDQ[31]	SDM[3]	SDQ[25]	SDQ[24]	SDQ[18]	SDQS[2]	SDQ[20]	SDQ[15]	SDQS[1]	SDQ[13]	SDQ[7]	SDQ[3]	NC	AH
AG	VCCSM	SDQ[58]	VSS	SDQ[60]	SDQ[55]	VSS	SDQ[52]	SDQ[47]	VSS	SDQ[41]	SDQ[39]	VSS	SDQ[33]	RSVD	VSS	RSVD	SDQ[26]	VSS	SDQ[28]	SDQ[19]	VSS	SDQ[17]	SDQ[10]	VSS	SDQ[9]	SDQ[6]	VSS	SDQS[0]	VCCSM	AG
AF	VCCSM	SDQ[59]	VCCSM	SDQ[61]	SDQ[54]	VCCSM	SDQ[53]	SDQ[42]	VCCSM	SDQ[44]	SDQ[34]	VCCSM	RSVD	RSVD	VCCSM	SDQ[27]	SDQ[30]	VCCSM	SMAB[4]	SDQ[22]	VCCSM	SDQ[16]	SDQ[14]	VCCSM	SDQ[12]	SDQ[2]	VCCSM	SDQ[0]	VCCASM	AF
AE	BCLK	VSS	SDQ[62]	SDQ[57]	VSS	SDQ[50]	SDQ[48]	VSS	SDQS[5]	SDQ[35]	VSS	SDQ[37]	RSVD	VSS	RSVD	RSVD	VSS	SDQS[3]	SDQ[23]	VSS	SDM[2]	SDQ[11]	VSS	SDM[1]	SDM[0]	VSS	SDQ[1]	SDQ[5]	VSS	AE
AD	BCLK#	RSTIN#	SDQ[63]	SCS[1]#	SWE#	SDM[6]	SCS[0]#	SBA[0]	SDM[5]	SBA[1]	SDM[4]	SDQ[36]	SMA[3]	SMAB[1]	SDQS[8]	SMA[1]	SMA[2]	SDQ[29]	SMA[4]	SMAB[5]	SDQ[21]	SMA[6]	SMA[7]	SDQ[8]	SMA[11]	SCK[2]#	SDQ[4]	SCK[3]#	VCCASM	AD
AC	VCCSM	VSS	VSS	SCK[1]	SCS[3]#	SCAS#	VSS	SCS[2]#	SRAS#	VSS	SMA[10]	SMA[0]	VSS	RCVENIN#	RCVENOUT	VSS	SMA[5]	SMAB[2]	VSS	SCKE[3]	SCKE[2]	VSS	SCKE[0]	SMA[8]	SMA[9]	VSS	SCK[2]	SCK[3]	VCCSM	AC
AB	VTTLF	HA[31]#	HA[29]#	VSS	SCK[1]#	SCK[4]#	SCK[4]	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	SCKE[1]	VCCSM	SMA[12]	SCK[5]#	VCCSM	SCK[0]	SMRCOMP	AB
AA	VSS	HA[27]#	HA[22]#	HADSTB[1]#	VSS	VSS	VSS	RSVD	VSS	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCCSM	VSS	VCCSM	VSS	NC	VCCSM	VSS	VCCSM	RSVD	VSS	SCK[5]	SCK[0]#	VSS	AA
Y	VTTLF	HCCVREF	HA[26]#	HA[30]#	HA[21]#	HA[17]#	DPSLP#	HAVREF	VSS												VCCSM	VSS	VCCSM	VSS	VSS	VCCSM	GCLKIN	VCCAGPLL	VCCHL	Y
W	VSS	HA[28]#	HA[25]#	VSS	HA[20]#	HA[23]#	HA[24]#	VSS	VCC												VSS	VCCHL	HL[7]	HL[5]	VCCHL	VSS	HLSTB	HL[4]	HLVREF	W
V	VTTHF	HA[11]#	HA[14]#	HA[16]#	HA[18]#	VSS	HA[19]#	VTTLF	VSS												VCCHL	VSS	VCCHL	HL[6]	HL[9]	HL[10]	HL[3]	HLSTB#	VCCHL	V
U	VSS	HA[10]#	HA[12]#	VSS	HA[15]#	HA[8]#	HA[7]#	VSS	VTTLF				VSS	VCC	VSS	VCC	VSS				VSS	VCCHL	HL[0]	VCCHL	VSS	HL[1]	HL[2]	PSWING	VSS	U
T		HA[5]#	HA[13]#	HADSTB[0]#	HA[4]#	VSS	HREQ[4]#	VTTLF	VSS				VCC	VSS	VCC	VSS	VCC				VSS	VSS	MDDCDATA	RSVD	RSVD	VSS	HL[8]	HLRCOMP		T
R		HREQ[0]#	HA[6]#	VSS	HREQ[3]#	HA[9]#	HREQ[2]#	VSS	VTTLF				VSS	VCC	VSS	VCC	VSS				VSS	VCCDVO	VSS	RSVD	RSVD	RSVD	RSVD	VSS		R
P		BPRI#	HLOCK#	RS[1]#	HREQ[1]#	VSS	HA[3]#	VTTLF	VSS				VCC	VSS	VCC	VSS	VCC				VCCDVO	VSS	MDDCCLK	RSVD	RSVD	RSVD	RSVD	RSVD		P
N	VSS	HITM#	HIT#	VSS	BNR#	DRDY#	RS[0]#	VSS	VTTLF				VSS	VCC	VSS	VCC	VSS				VSS	VCCDVO	MDVICLK	MI2CDATA	RSVD	VSS	RSVD	RSVD	VCCDVO	N
M	VTTHF	DEFER#	RS[2]#	DBSY#	HTRDY#	VSS	BREQ0#	VTTLF	VSS												VCCDVO	VCCDVO	VSS	MDVIDATA	RSVD	VCCDVO	DVOBCCLKINT	RSVD	RSVD	M
L	VSS	ADS#	HD[6]#	VSS	HD[8]#	HD[3]#	HD[7]#	VSS	VTTLF												VSS	VCCDVO	DVODETECT	VSS	DVOCVSYNC	RSVD	DVOCBLANK#	RSVD	VSS	L
K	VTTLF	HYSWING	HDSTBP[0]#	HD[13]#	HD[2]#	VSS	HD[11]#	HD[0]#	HDVREF												VCCDVO	VSS	MI2CCLK	DVOCHSYNC	DVOCD[0]	VSS	DVOCD[2]	DVOCD[3]	DVOCD[1]	K
J	VSS	HDSTBN[0]#	HD[4]#	VSS	DINV[0]#	HD[9]#	HD[14]#	VSS	HDVREF[1]	VSS	VTTLF	VSS	HDVREF[2]	VSS	VCC	VSS	VCC1_5	VSS	PWROK	VSS	VSYNC	VCCDVO	VSS	DVOCD[4]	DVOCD[5]	VCCDVO	DVOCCLK	DVOCCLK#	VCCDVO	J
H	VTTHF	HYRCOMP	HD[1]#	HD[15]#	HD[10]#	VSS	HD[19]#	VTTLF	VSS	VTTLF	VSS	VTTLF	VSS	VTTLF	VSS	VCC	VSS	RSVD	VSS	HSYNC	LCLKCTLA	VSS	VCCDVO	DVOCD[10]	DVOCFLDSTL	DVOCD[9]	DVOCD[8]	DVOCD[6]	DVOCD[7]	H
G	VSS	HD[5]#	HD[12]#	VSS	HD[21]#	HD[24]#	HD[30]#	HD[27]#	HD[33]#	HD[40]#	DINV[3]#	HD[48]#	HD[51]#	HD[58]#	VTTLF	RSVD	VCC1_5	RSVD	RSVD	RSVD	DDCADATA	RSVD	VSS	ADDID[6]	ADDID[4]	VSS	DVOCD[11]	DVOBCINTR#	VSS	G
F	VTTLF	HD[22]#	VSS	HD[17]#	HD[16]#	VSS	HD[44]#	VSS	HD[45]#	VSS	HD[53]#	VSS	HD[56]#	VSS	CPURST#	RSVD	VSS	RSVD	VSS	RSVD	VCC2_5	RSVD	RSVD	ADDID[7]	ADDID[1]	ADDID[5]	RSVD	RSVD	GVREF	F
E	VSS	VSS	HD[20]#	HD[29]#	DINV[1]#	HD[38]#	HD[41]#	HDSTBN[2]#	HDSTBP[2]#	HD[50]#	HD[49]#	HDSTBP[3]#	HD[61]#	HD[59]#	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	VSS	REFSET	VSS	VCCDVO	ADDID[0]	VCCDVO	ADDID[2]	ADDID[3]	VCCDVO	E
D	VCCAHPLL	VSS	HD[23]#	HDSTBP[1]#	VSS	HD[39]#	VSS	HD[36]#	VSS	HD[52]#	VSS	HDSTBN[3]#	VSS	HD[62]#	VSS	RSVD	VSS	RSVD	VSS	VCC2_5	BLUE#	GREEN#	RSVD	EXTTS_0	DPMS	VSS	RSVD	RSVD	DVORCOMP	D
C	VSS	HD[25]#	HDSTBN[1]#	HD[28]#	HD[37]#	HD[34]#	HD[35]#	VSS	HD[47]#	HD[46]#	HD[54]#	HD[63]#	HD[55]#	HD[60]#	RSVD	RSVD	RSVD	RSVD	RSVD	VSS	BLUE	GREEN	VSS	LCLKCTLB	RSVD	GST[0]	GST[1]	GST[2]	VSS	C
B	NC	HD[31]#	HD[18]#	HD[26]#	DINV[2]#	VSS	HD[43]#	HD[42]#	HD[32]#	HXRCOMP	HD[57]#	HXSWING	RSVD	VCCADPLLB	VCC1_5	VCC1_5	RSVD	RSVD	VSSA	VCC2_5	VCCADAC	VSSADAC	DREFCLK	DDCACLK	VSS	RSVD	RSVD	RSVD	NC	B
A	NC	NC	VSS	VTTLF	VSS	VTTHF	VSS	VTTHF	VSS	VTTLF	VSS	VTTLF	VSS				VSS	VCC2_5	VCCA	RSVD	VCCADAC	RED#	RED	VCCADPLLA	RSVD	VCCGPIO	VCCGPIO	NC		A
	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

9.1 VCC/VSS Voltage Groups

Table 35. Voltage Levels and Ball Out for Voltage Groups

Name	Voltage Level	Ball out
VCC	1.5	H14,J15,N14,N16,P13,P15,P17,R14,R16,T13,T15, T17,U14,U16,W21,AA15,AA17,AA19
VCCADAC	1.5	A9,B9
VCCDVO	1.5	E1,E4,E6,H7,J1,J4,J8,K9,L8,M4,M8,M9,N1,N8,P9,R8
VCCASM	1.5	AD1,AF1
VCC1_5	1.5	B14,B15,G13,J13
VCCGPIO	3.3	A3,A4
VCCHL	1.5	U6,U8,V1,V7,V9,W5,W8,Y1
VCCQSM	2.5	AJ6,AJ8
VCCSM	2.5	Y4,Y7,Y9,AA6,AA8,AA11,AA13,AB3,AB6,AB8,AB10, AB12,AB14,AB16,AB18,AB20,AB22,AC1,AC29,AF3, AF6,AF9,AF12,AF15,AF18,AF21,AF24,AF27,AF29, AG1,AG29,AJ5,AJ9,AJ13,AJ17,AJ21,AJ25
VCC2_5	2.5	A12,B10,D10,F9
VTTHF	1.5	A22,A24,H29,M29,V29
VTTLF	1.5	A18,A20,A26,F29,G15,H16,H18,H20,H22,J19,K29,L21, M22,N21,P22,R21,T22,U21,V22,Y29,AB29
VSS	GND	A13,A17,A19,A21,A23,A25,A27,B5,B24,C1,C7,C10,C22,C29, D4,D11,D13,D15,D17,D19,D21,D23,D25,D28,E7,E9,E28,E29, F11,F13,F16,F18,F20,F22,F24,F27,G1,G4,G7,G26,G29,H8,H11, H13,H15,H17,H19,H21,H24,J7,J10,J12,J14,J16,J18,J20,J22,J26, J29,K4,K8,K24,L1,L6,L9,L22,L26,L29,M7,M21,M24,N4,N9,N13, N15,N17,N22,N26,N29,P8,P14,P16,P21,P24,R2,R7,R9,R13,R15, R17,R22,R26,T4,T8,T9,T14,T16,T21,T24,U1,U5,U9,U13,U15, U17,U22,U26,U29,V8,V21,V24,W4,W9,W22,W26,W29,Y5,Y6, Y8,Y21,AA1,AA4,AA7,AA10,AA12,AA14,AA16,AA18,AA20, AA21,AA23,AA24,AA25,AA29,AB9,AB11,AB13,AB15,AB17, AB19,AB21,AB26,AC4,AC8,AC11,AC14,AC17,AC20,AC23, AC27,AC28,AE1,AE4,AE7,AE10,AE13,AE16,AE19,AE22,AE25, AE28,AG3,AG6,AG9,AG12,AG15,AG18,AG21,AG24,AG27,AJ1, AJ3,AJ7,AJ10,AJ11,AJ12,AJ18,AJ20,AJ23,AJ26,AJ27

Table 36. Ballout Table

Row	Column	Signal Name	Row	Column	Signal Name	Row	Column	Signal Name
E	5	ADDID[0]	AA	22	DPWR#	G	3	DVOCD[11]
F	5	ADDID[1]	N	24	DRDY#	K	3	DVOCD[2]
E	3	ADDID[2]	B	7	DREFCLK	K	2	DVOCD[3]
E	2	ADDID[3]	B	17	RSVD	J	6	DVOCD[4]
G	5	ADDID[4]	L	2	DVOBBLANK#	J	5	DVOCD[5]
F	4	ADDID[5]	M	3	DVOBCCLKINT	H	2	DVOCD[6]
G	6	ADDID[6]	G	2	DVOBCINTR#	H	1	DVOCD[7]
F	6	ADDID[7]	P	3	DVOBCLK	H	3	DVOCD[8]
L	28	ADS#	P	4	DVOBCLK#	H	4	DVOCD[9]
F	7	RSVD	R	3	DVOBD[0]	H	5	DVOCFLDSTL
AE	29	BCLK	R	5	DVOBD[1]	K	6	DVOCHSYNC
AD	29	BCLK#	M	1	DVOBD[10]	L	5	DVOCVSYNC
C	9	BLUE	M	5	DVOBD[11]	L	7	DVODETECT
D	9	BLUE#	R	6	DVOBD[2]	D	1	DVORCOMP
N	25	BNR#	R	4	DVOBD[3]	D	6	EXTTS_0
P	28	BPRI#	P	6	DVOBD[4]	Y	3	GCLKIN
M	23	BREQ0#	P	5	DVOBD[5]	C	8	GREEN
F	15	CPURST#	N	5	DVOBD[6]	D	8	GREEN#
M	26	DBSY#	P	2	DVOBD[7]	F	1	GVREF
B	6	DDCACLK	N	2	DVOBD[8]	U	28	HA[10]#
G	9	DDCADATA	N	3	DVOBD[9]	V	28	HA[11]#
B	4	RSVD	M	2	DVOBFLDSTL	U	27	HA[12]#
C	5	RSVD	T	6	DVOBHSYNC	T	27	HA[13]#
M	28	DEFER#	T	5	DVOBVSYNC	V	27	HA[14]#
J	25	DINV[0]#	L	3	DVOCBLANK#	U	25	HA[15]#
E	25	DINV[1]#	J	3	DVOCCLK	V	26	HA[16]#
B	25	DINV[2]#	J	2	DVOCCLK#	Y	24	HA[17]#
G	19	DINV[3]#	K	5	DVOCD[0]	V	25	HA[18]#
D	5	DPMS	K	1	DVOCD[1]	V	23	HA[19]#
Y	23	DPSLP#	H	6	DVOCD[10]	W	25	HA[20]#

Row	Column	Signal Name	Row	Column	Signal Name	Row	Column	Signal Name
Y	25	HA[21]#	F	25	HD[16]#	B	23	HD[43]#
AA	27	HA[22]#	F	26	HD[17]#	F	23	HD[44]#
W	24	HA[23]#	B	27	HD[18]#	F	21	HD[45]#
W	23	HA[24]#	H	23	HD[19]#	C	20	HD[46]#
W	27	HA[25]#	K	25	HD[2]#	C	21	HD[47]#
Y	27	HA[26]#	E	27	HD[20]#	G	18	HD[48]#
AA	28	HA[27]#	G	25	HD[21]#	E	19	HD[49]#
W	28	HA[28]#	F	28	HD[22]#	G	28	HD[5]#
AB	27	HA[29]#	D	27	HD[23]#	E	20	HD[50]#
P	23	HA[3]#	G	24	HD[24]#	G	17	HD[51]#
Y	26	HA[30]#	C	28	HD[25]#	D	20	HD[52]#
AB	28	HA[31]#	B	26	HD[26]#	F	19	HD[53]#
T	25	HA[4]#	G	22	HD[27]#	C	19	HD[54]#
T	28	HA[5]#	C	26	HD[28]#	C	17	HD[55]#
R	27	HA[6]#	E	26	HD[29]#	F	17	HD[56]#
U	23	HA[7]#	L	24	HD[3]#	B	19	HD[57]#
U	24	HA[8]#	G	23	HD[30]#	G	16	HD[58]#
R	24	HA[9]#	B	28	HD[31]#	E	16	HD[59]#
T	26	HADSTB[0]#	B	21	HD[32]#	L	27	HD[6]#
AA	26	HADSTB[1]#	G	21	HD[33]#	C	16	HD[60]#
Y	22	HAVREF	C	24	HD[34]#	E	17	HD[61]#
Y	28	HCCVREF	C	23	HD[35]#	D	16	HD[62]#
K	22	HD[0]#	D	22	HD[36]#	C	18	HD[63]#
H	27	HD[1]#	C	25	HD[37]#	L	23	HD[7]#
H	25	HD[10]#	E	24	HD[38]#	L	25	HD[8]#
K	23	HD[11]#	D	24	HD[39]#	J	24	HD[9]#
G	27	HD[12]#	J	27	HD[4]#	J	28	HDSTBN[0]#
K	26	HD[13]#	G	20	HD[40]#	C	27	HDSTBN[1]#
J	23	HD[14]#	E	23	HD[41]#	E	22	HDSTBN[2]#
H	26	HD[15]#	B	22	HD[42]#	D	18	HDSTBN[3]#

Row	Column	Signal Name	Row	Column	Signal Name	Row	Column	Signal Name
K	27	HDSTBP[0]#	H	10	HSYNC	T	7	MDDCDATA
D	26	HDSTBP[1]#	M	25	HTRDY#	N	7	MDVICLK
E	21	HDSTBP[2]#	B	20	HXRCOMP	M	6	MDVIDATA
E	18	HDSTBP[3]#	B	18	HXSWING	K	7	MI2CCLK
K	21	HDVREF[0]	H	28	HYRCOMP	N	6	MI2CDATA
J	21	HDVREF[1]	K	28	HYSWING	AJ	29	NC
J	17	HDVREF[2]	D	14	RSVD	AH	29	NC
N	27	HIT#	E	13	RSVD	B	29	NC
N	28	HITM#	E	10	RSVD	A	29	NC
U	7	HL[0]	F	10	RSVD	AJ	28	NC
U	4	HL[1]	G	14	RSVD	A	28	NC
V	4	HL[10]	E	15	RSVD	AA	9	NC
U	3	HL[2]	C	15	RSVD	AJ	4	NC
V	3	HL[3]	C	13	RSVD	AJ	2	NC
W	2	HL[4]	F	14	RSVD	A	2	NC
W	6	HL[5]	E	14	RSVD	AH	1	NC
V	6	HL[6]	C	14	RSVD	B	1	NC
W	7	HL[7]	B	13	RSVD	G	8	RSVD
T	3	HL[8]	H	12	RSVD	F	8	RSVD
V	5	HL[9]	E	12	RSVD	A	5	RSVD
P	27	HLOCK#	C	12	RSVD	U	2	PSWING
T	2	HLRCOMP	G	11	RSVD	J	11	PWROK
W	3	HLSTB	G	12	RSVD	AC	16	RCVENIN#
V	2	HLSTB#	E	11	RSVD	AC	15	RCVENOUT#
W	1	HLVREF	C	11	RSVD	A	7	RED
R	28	HREQ[0]#	G	10	RSVD	A	8	RED#
P	25	HREQ[1]#	H	9	LCLKCTLA	E	8	REFSET
R	23	HREQ[2]#	C	6	LCLKCTLB	N	23	RS[0]#
R	25	HREQ[3]#	A	10	RSVD	P	26	RS[1]#
T	23	HREQ[4]#	P	7	MDDCCLK	M	27	RS[2]#

Row	Column	Signal Name	Row	Column	Signal Name	Row	Column	Signal Name
AD	28	RSTIN#	AB	4	SCK[5]#	AF	4	SDQ[2]
F	12	RSVD	AC	7	SCKE[0]	AH	7	SDQ[20]
D	12	RSVD	AB	7	SCKE[1]	AD	9	SDQ[21]
B	12	RSVD	AC	9	SCKE[2]	AF	10	SDQ[22]
AA	5	RSVD	AC	10	SCKE[3]	AE	11	SDQ[23]
L	4	RSVD	AD	23	SCS[0]#	AH	10	SDQ[24]
C	4	GST[0]	AD	26	SCS[1]#	AH	11	SDQ[25]
F	3	RSVD	AC	22	SCS[2]#	AG	13	SDQ[26]
D	3	RSVD	AC	25	SCS[3]#	AF	14	SDQ[27]
C	3	GST[1]	AE	5	SDM[0]	AG	11	SDQ[28]
B	3	RSVD	AE	6	SDM[1]	AD	12	SDQ[29]
F	2	RSVD	AE	9	SDM[2]	AH	2	SDQ[3]
D	2	RSVD	AH	12	SDM[3]	AF	13	SDQ[30]
C	2	GST[2]	AD	19	SDM[4]	AH	13	SDQ[31]
B	2	RSVD	AD	21	SDM[5]	AH	16	SDQ[32]
D	7	RSVD	AD	24	SDM[6]	AG	17	SDQ[33]
AD	22	SBA[0]	AH	28	SDM[7]	AF	19	SDQ[34]
AD	20	SBA[1]	AH	15	SDM[8]	AE	20	SDQ[35]
AC	24	SCAS#	AF	2	SDQ[0]	AD	18	SDQ[36]
AB	2	SCK[0]	AE	3	SDQ[1]	AE	18	SDQ[37]
AA	2	SCK[0]#	AG	7	SDQ[10]	AH	18	SDQ[38]
AC	26	SCK[1]	AE	8	SDQ[11]	AG	19	SDQ[39]
AB	25	SCK[1]#	AF	5	SDQ[12]	AD	3	SDQ[4]
AC	3	SCK[2]	AH	4	SDQ[13]	AH	20	SDQ[40]
AD	4	SCK[2]#	AF	7	SDQ[14]	AG	20	SDQ[41]
AC	2	SCK[3]	AH	6	SDQ[15]	AF	22	SDQ[42]
AD	2	SCK[3]#	AF	8	SDQ[16]	AH	22	SDQ[43]
AB	23	SCK[4]	AG	8	SDQ[17]	AF	20	SDQ[44]
AB	24	SCK[4]#	AH	9	SDQ[18]	AH	19	SDQ[45]
AA	3	SCK[5]	AG	10	SDQ[19]	AH	21	SDQ[46]

Row	Column	Signal Name	Row	Column	Signal Name	Row	Column	Signal Name
AG	22	SDQ[47]	AG	2	SDQS[0]	AC	21	SRAS#
AE	23	SDQ[48]	AH	5	SDQS[1]	AD	25	SWE#
AH	23	SDQ[49]	AH	8	SDQS[2]	W	21	VCC
AE	2	SDQ[5]	AE	12	SDQS[3]	AA	19	VCC
AE	24	SDQ[50]	AH	17	SDQS[4]	AA	17	VCC
AH	25	SDQ[51]	AE	21	SDQS[5]	T	17	VCC
AG	23	SDQ[52]	AH	24	SDQS[6]	P	17	VCC
AF	23	SDQ[53]	AH	27	SDQS[7]	U	16	VCC
AF	25	SDQ[54]	AD	15	SDQS[8]	R	16	VCC
AG	25	SDQ[55]	AC	18	SMA[0]	N	16	VCC
AH	26	SDQ[56]	AD	14	SMA[1]	AA	15	VCC
AE	26	SDQ[57]	AC	19	SMA[10]	T	15	VCC
AG	28	SDQ[58]	AD	5	SMA[11]	P	15	VCC
AF	28	SDQ[59]	AB	5	SMA[12]	J	15	VCC
AG	4	SDQ[6]	AD	13	SMA[2]	U	14	VCC
AG	26	SDQ[60]	AD	17	SMA[3]	R	14	VCC
AF	26	SDQ[61]	AD	11	SMA[4]	N	14	VCC
AE	27	SDQ[62]	AC	13	SMA[5]	H	14	VCC
AD	27	SDQ[63]	AD	8	SMA[6]	T	13	VCC
AG	14	RSVD	AD	7	SMA[7]	P	13	VCC
AE	14	RSVD	AC	6	SMA[8]	B	9	VCCADAC
AE	17	RSVD	AC	5	SMA[9]	A	9	VCCADAC
AG	16	RSVD	AD	16	SMAB[1]	A	6	VCCADPLLA
AH	14	RSVD	AC	12	SMAB[2]	B	16	VCCADPLLB
AE	15	RSVD	AF	11	SMAB[4]	Y	2	VCCAGPLL
AH	3	SDQ[7]	AD	10	SMAB[5]	D	29	VCCAHPLL
AF	16	RSVD	AB	1	SMRCOMP	A	11	VCCA
AF	17	RSVD	AJ	24	SMVREF_0	AF	1	VCCASM
AD	6	SDQ[8]	AJ	19	SMVSWINGH	AD	1	VCCASM
AG	5	SDQ[9]	AJ	22	SMVSWINGL	B	15	VCC1_5

Row	Column	Signal Name	Row	Column	Signal Name	Row	Column	Signal Name
B	14	VCC1_5	AJ	6	VCCQSM	AB	6	VCCSM
J	13	VCC1_5	AG	29	VCCSM	AA	6	VCCSM
G	13	VCC1_5	AF	29	VCCSM	AJ	5	VCCSM
P	9	VCCDVO	AC	29	VCCSM	Y	4	VCCSM
M	9	VCCDVO	AF	27	VCCSM	AF	3	VCCSM
K	9	VCCDVO	AJ	25	VCCSM	AB	3	VCCSM
R	8	VCCDVO	AF	24	VCCSM	AG	1	VCCSM
N	8	VCCDVO	AB	22	VCCSM	AC	1	VCCSM
M	8	VCCDVO	AJ	21	VCCSM	A	12	VCC2_5
L	8	VCCDVO	AF	21	VCCSM	D	10	VCC2_5
J	8	VCCDVO	AB	20	VCCSM	B	10	VCC2_5
H	7	VCCDVO	AF	18	VCCSM	F	9	VCC2_5
E	6	VCCDVO	AB	18	VCCSM	AA	29	VSS
M	4	VCCDVO	AJ	17	VCCSM	W	29	VSS
J	4	VCCDVO	AB	16	VCCSM	U	29	VSS
E	4	VCCDVO	AF	15	VCCSM	N	29	VSS
N	1	VCCDVO	AB	14	VCCSM	L	29	VSS
J	1	VCCDVO	AJ	13	VCCSM	J	29	VSS
E	1	VCCDVO	AA	13	VCCSM	G	29	VSS
A	4	VCCGPIO	AF	12	VCCSM	E	29	VSS
A	3	VCCGPIO	AB	12	VCCSM	C	29	VSS
V	9	VCCHL	AA	11	VCCSM	AE	28	VSS
W	8	VCCHL	AB	10	VCCSM	AC	28	VSS
U	8	VCCHL	AJ	9	VCCSM	E	28	VSS
V	7	VCCHL	AF	9	VCCSM	D	28	VSS
U	6	VCCHL	Y	9	VCCSM	AJ	27	VSS
W	5	VCCHL	AB	8	VCCSM	AG	27	VSS
Y	1	VCCHL	AA	8	VCCSM	AC	27	VSS
V	1	VCCHL	Y	7	VCCSM	F	27	VSS
AJ	8	VCCQSM	AF	6	VCCSM	A	27	VSS

Row	Column	Signal Name	Row	Column	Signal Name	Row	Column	Signal Name
AJ	26	VSS	U	22	VSS	AA	18	VSS
AB	26	VSS	R	22	VSS	J	18	VSS
W	26	VSS	N	22	VSS	F	18	VSS
U	26	VSS	L	22	VSS	AC	17	VSS
R	26	VSS	J	22	VSS	AB	17	VSS
N	26	VSS	F	22	VSS	U	17	VSS
L	26	VSS	C	22	VSS	R	17	VSS
J	26	VSS	AG	21	VSS	N	17	VSS
G	26	VSS	AB	21	VSS	H	17	VSS
AE	25	VSS	AA	21	VSS	D	17	VSS
AA	25	VSS	Y	21	VSS	A	17	VSS
D	25	VSS	V	21	VSS	AE	16	VSS
A	25	VSS	T	21	VSS	AA	16	VSS
AG	24	VSS	P	21	VSS	T	16	VSS
AA	24	VSS	M	21	VSS	P	16	VSS
V	24	VSS	H	21	VSS	J	16	VSS
T	24	VSS	D	21	VSS	F	16	VSS
P	24	VSS	A	21	VSS	AG	15	VSS
M	24	VSS	AJ	20	VSS	AB	15	VSS
K	24	VSS	AC	20	VSS	U	15	VSS
H	24	VSS	AA	20	VSS	R	15	VSS
F	24	VSS	J	20	VSS	N	15	VSS
B	24	VSS	F	20	VSS	H	15	VSS
AJ	23	VSS	AE	19	VSS	D	15	VSS
AC	23	VSS	AB	19	VSS	AC	14	VSS
AA	23	VSS	H	19	VSS	AA	14	VSS
D	23	VSS	D	19	VSS	T	14	VSS
A	23	VSS	A	19	VSS	P	14	VSS
AE	22	VSS	AJ	18	VSS	J	14	VSS
W	22	VSS	AG	18	VSS	AE	13	VSS

Row	Column	Signal Name	Row	Column	Signal Name	Row	Column	Signal Name
AB	13	VSS	L	9	VSS	K	4	VSS
U	13	VSS	E	9	VSS	G	4	VSS
R	13	VSS	AC	8	VSS	D	4	VSS
N	13	VSS	Y	8	VSS	AJ	3	VSS
H	13	VSS	V	8	VSS	AG	3	VSS
F	13	VSS	T	8	VSS	R	2	VSS
D	13	VSS	P	8	VSS	AJ	1	VSS
A	13	VSS	K	8	VSS	AE	1	VSS
AJ	12	VSS	H	8	VSS	AA	1	VSS
AG	12	VSS	AJ	7	VSS	U	1	VSS
AA	12	VSS	AE	7	VSS	L	1	VSS
J	12	VSS	AA	7	VSS	G	1	VSS
AJ	11	VSS	R	7	VSS	C	1	VSS
AC	11	VSS	M	7	VSS	B	8	VSSADAC
AB	11	VSS	J	7	VSS	B	11	VSSA
H	11	VSS	G	7	VSS	J	9	VSYNC
F	11	VSS	E	7	VSS	V	29	VTTHF
D	11	VSS	C	7	VSS	M	29	VTTHF
AJ	10	VSS	AG	6	VSS	H	29	VTTHF
AE	10	VSS	Y	6	VSS	A	24	VTTHF
AA	10	VSS	L	6	VSS	A	22	VTTHF
J	10	VSS	Y	5	VSS	AB	29	VTTLF
C	10	VSS	U	5	VSS	Y	29	VTTLF
AG	9	VSS	B	5	VSS	K	29	VTTLF
AB	9	VSS	AE	4	VSS	F	29	VTTLF
W	9	VSS	AC	4	VSS	A	26	VTTLF
U	9	VSS	AA	4	VSS	V	22	VTTLF
T	9	VSS	W	4	VSS	T	22	VTTLF
R	9	VSS	T	4	VSS	P	22	VTTLF
N	9	VSS	N	4	VSS	M	22	VTTLF

Row	Column	Signal Name
H	22	VTTLF
U	21	VTTLF
R	21	VTTLF
N	21	VTTLF
L	21	VTTLF
H	20	VTTLF
A	20	VTTLF
J	19	VTTLF
H	18	VTTLF
A	18	VTTLF
H	16	VTTLF
G	15	VTTLF

9.2 Package Mechanical Information

Figure 13 through Figure 15 provide detail on the package information and dimensions of the Intel® 82854 GMCH. The Intel® 82854 GMCH comes in a Micro-FCBGA package, which is similar to the mobile processors. The package consists of a silicon die mounted face down on an organic substrate populated with solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keepout area, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

Figure 13. Intel® 82854 GMCH Micro-FCBGA Package Dimensions (Top View)

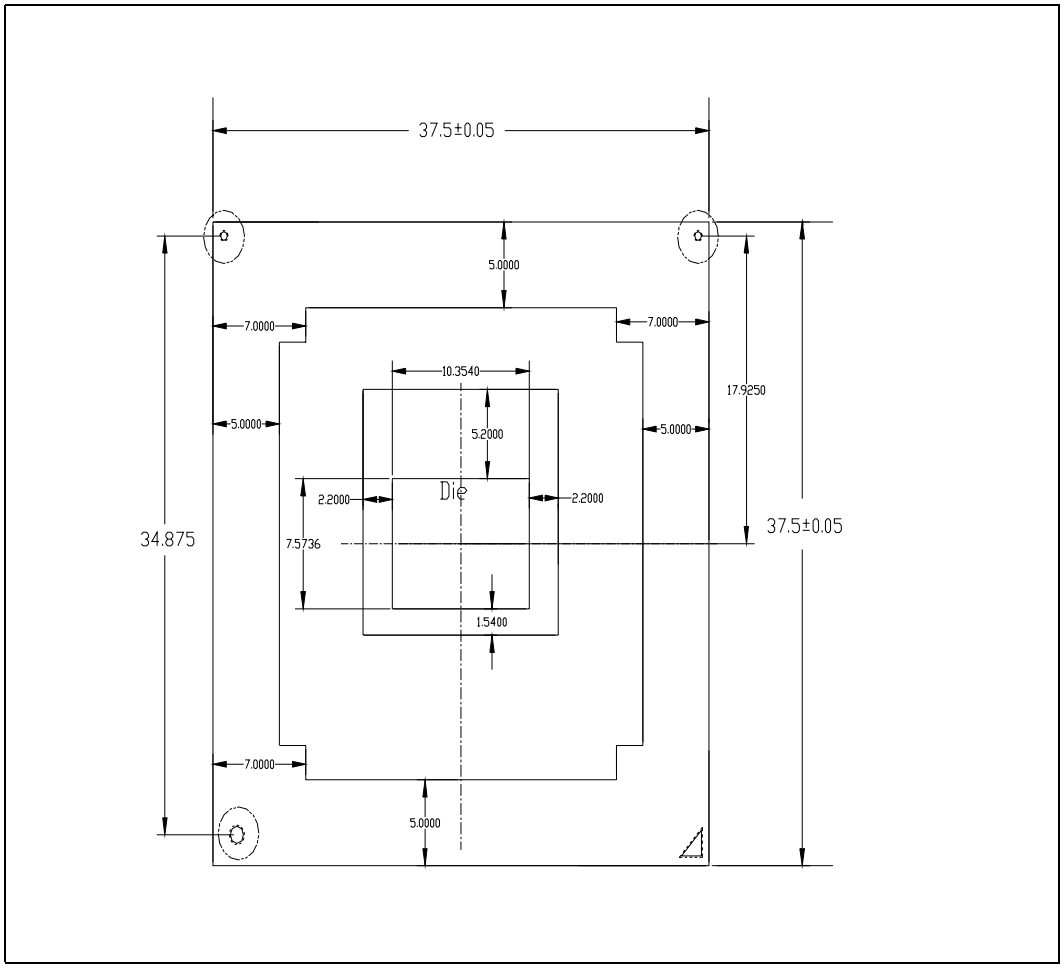


Figure 14. Intel® 82854 GMCH Micro-FCBGA Package Dimensions (Side View)

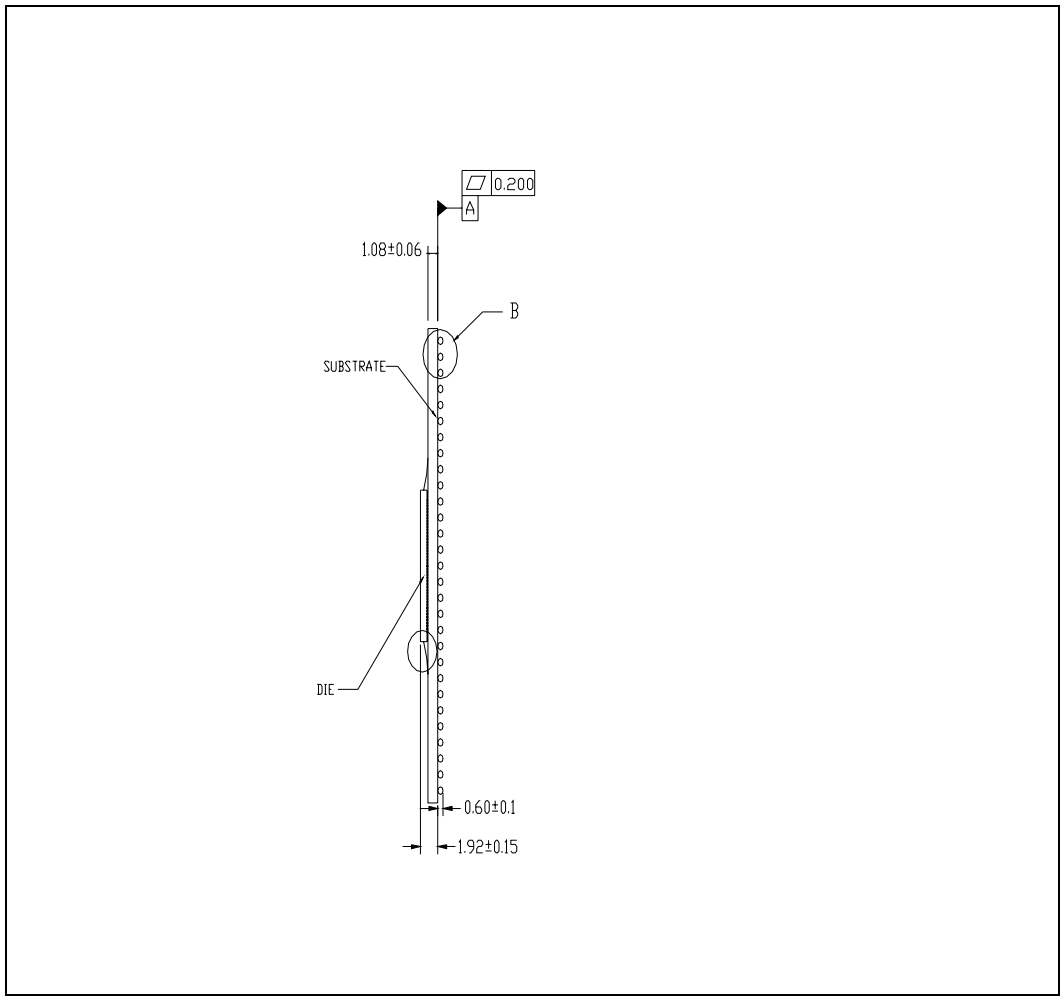


Figure 15. Intel® 82854 GMCH Micro-FCBGA Package Dimensions (Bottom View)